A study of ultrahigh speed optical integrated circuits on Si substrate

Doctoral dissertation

A study of ultrahigh speed
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ABSTRACT

Nowadays, everyone around the world can enjoy themselves by sharing amount of transmitted data, thanks to the large-volume optical fiber transmissions have been widespread in the long-haul communication systems since 1980s. Recently, given a dramatically increasing of the data traffic, at a compound annual growth rate of 40% or even more, in the short-distance communications such as rack-to-rack, board-to-board and chip-to-chip, the optical communications have also been introduced gradually instead of traditional electrical communications, namely, optical interconnections.

Especially, given an integrated circuit of a large-volume optical interface to a high-performance electrical LSI processing is proposed to lead a generational communication system. In order to enable a cost-effective implementation of this optical short-distance connections, a complementary metal-oxide-semiconductor (CMOS) compatible process is an useful, low-cost approach for a monolithic integration of available, complex, and high-speed optical circuits, combining with general 850 nm transmitters and platform Si photodetectors to form an optoelectronic integrated circuit (OEIC) on a Si substrate.

This study was carried out to realize an active optical cable (AOC) integrated with Si-LSIs, proposed by an optical integrated circuit of a low-loss high-refractive-index tantalum pentoxide (Ta_2O_5) waveguide and an ultra-high speed Si-PIN photodetector (Si-PIN PD), utilizing a directional waveguide grating coupler in the 0.8 μm wavelength range. Firstly, the high-refractive-index (n ~2.0) and low propagation loss (< 1 dB/cm) Ta_2O_5 waveguide with a cross section of 400 nm x 10 μm was fabricated by a chemical solution deposition followed by a CF_4 reactive ion dry etching. Secondly, the directional waveguide grating coupler was calculated by using finite element method (FEM) to achieve a bottom directional coupling efficiency > 60% with a grating length of 15 μm, at a grating period of 530 nm, a duty ratio of 0.5, and an etching depth ratio > 0.9 with a thickness of 400 nm. Finally, the lateral Si-PIN PDs fabricated on an silicon-on-insulator (SOI) substrate (absorber layer thickness of 210 nm) in the CMOS compatible process were designed and implemented with a finger width of 1.00 μm, a finger spacing of 1.63 μm, a square detector area of 20 × 20 μm^2, and a pad size of 30 × 30 μm^2. A bandwidth of 13.6 GHz was obtained at a bias voltage of 10 V at 850 nm wavelength.

In a word, these technologies can be expected to realize an OEIC on Si-LSIs in the 0.8 μm wavelength range as a cost-effective implementation.

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Introduction

1.1 Motivation

1.1.1 From long-haul optical fiber communications to short-distance optical interconnects

1.1.1.1 Development of fibers and lasers for long-haul optical communication systems

The practical research of optical communication systems was started from 1962, since the first realization of a gallium arsenide (GaAs) semiconductor laser diode emitting in 0.8 μm wavelength range [1, 2]. However, propagation of light, even a laser light, in free-space cannot be reliably used, due to the significant wave diffraction and the dependence of the attenuation on atmospheric conditions. Therefore, a guided propagation of light was studied on the optical fiber. Since 1970, *Corning Glass Works* had reported an optical fiber with 20 decibels per kilometer (dB/km) loss by a chemical vapor deposition (CVD) method [3].

Bell Laboratory developed an optical fiber with 2.5 dB/km loss using a modified chemical vapor deposition (MCVD) method in 1974 [4]. *Nippon Telegraph and Telephone Corporation* and *Fujikura Ltd.* achieved attenuation of 0.47 dB/km in 1.2 μm wavelength in 1976, and later 0.20 dB/km in 1.55 μm wavelength in 1979 [5]. The propagation loss of a glass optical fiber had been developed to one-hundredth of the value in the 1970s. For the improvement of optical fiber technology, *Sumitomo Electric Industries Ltd.* reported on a pure silica core fiber with ultra-low loss of 0.154 dB/km in 1986 [6] and the propagation loss of optical fiber was thought to come close to the clarity limit. Newsletters introduce optical fibers with the record-breaking low loss of 0.151 dB/km at the OFC2002 [7] and further improved loss of 0.1484 dB/km in the Electronics Letters [8].

Simultaneously, the development of room-temperature (RT) continuous-wave (CW) operated semiconductor lasers is very promising in relation to progress on optical communication systems. In 1970, the first RT CW operated edge-emitting semiconductor laser was developed by using a double-heterostructure in a GaAs/AlGaAs material system [9, 10]. Then, the first experimental demonstration of a Raman fiber amplifier in 1973 [11], the first RT CW semiconductor diode distributed-feedback (DFB) laser in

1975 [12], and the first CW InGaAsP laser in 1976 [13] were reported serially. These lasers have been widely used for telecommunication networks ranging from backbone to access networks. What's more, the implementation of single mode lasers [14, 15] in early 1980s led to high speed direct modulation of the laser becoming possible.

Particularly, in 1979, a AsP/InP surface emitting semiconductor lasers, utilizing an invention of a vertical cavity surface emitting laser (VCSEL) structure by *H. Soda et al.* was reported, and the CW operation of the VCSEL was demonstrated at RT in a GaAs material system in 1989 [16]. As some important breakthroughs, the first realization of a Ti-Sapphire laser by *Peter F. Moulton* in 1986 [17], an erbium-doped fiber amplifier (EDFA) for optical communications was realized by *R. J. Mears et al.* in 1987 [18], and a quantum cascade laser (QCL) was invented and demonstrated by *F. Capasso et al.* in1994 [19], and then GaN and InGaN semiconductor lasers by *S. Nakamura et al.* in 1996 [20]. Semiconductor lasers have mentioned overthinking achievement during this half of 20 century.

1.1.1.2 Applications of optical fiber communications in the real world

As the first commercial application of optical communication systems, in 1977, both *AT&T* and *GTE* introduced fiber optic-telephone system in *Chicago* and *Boston*, respectively. By the early 1980s, single mode fiber operating in the 1310 nm, and later the 1550 nm wavelength windows became the standard fiber installed for these networks. Initially, computers, information networks, and data transmissions were slower to embrace fibers, but today they are found extra useful for a communication system that has lighter weight cables, resists lightning strikes, and carries more information faster and over longer distances. In this way, the optical fiber communication systems were used practically in worldwide since around 1980s. Simultaneously, the time division multiplexing (TDM) of optical fiber communication systems by 32 Mbps, 100 Mbps method were introduced firstly as a commercial application from 1981 in Japan [21]. Especially, *Bell Laboratory* transmitted a 2.5 gigabits per second (Gbps) signal over 7,500 km without regeneration in 1990. The system used a solation laser and an EDFA that allowed the lightwave to maintain its shape and density. It was a major breakthrough for the implementation of advanced optical fiber communication system utilizing wavelength division multiplexing (WDM) technology. Since then on, in 1998, it went one better level by researchers in North America transmitted 100 simultaneous optical signals, each at a data rate of 10 Gbps for a long distance of nearly 250 miles (400 km). In this experiment, dense wavelength-division multiplexing (DWDM) technology combined with TDM utilizing vestigial side band (VSB) or single side band (SSB) modulation

scheme practical application was progress, which allows multiple wavelengths to be combined into one optical signal, improving frequency utilization efficiency, and significantly increased the total data rate on one fiber to one terabit per second (Tbps, means 10^{12} bits per second) [22].

In the case of Japan, WDM communication scheme has widely introduced into not only a local area network (LAN) but also a metropolitan area network (MAN) since around 2000. Even a further access network, employing fiber to the home (FTTH), it is possible to draw a low-cost optical fiber communicate to common Japanese household, and a high channel capacity of over 100 Mbps came to be familiar at the lowest cost in the world. The historical improvement of total optical fiber capacity is shown in Fig. 1-1.

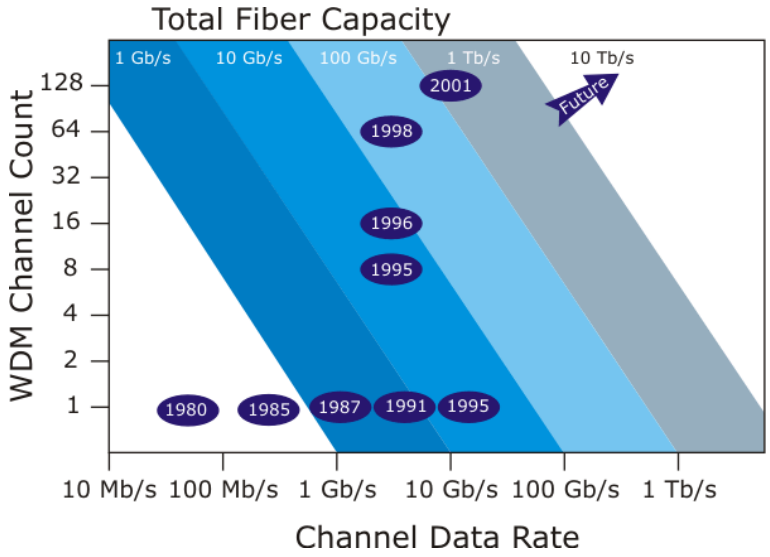


Fig. 1-1 A historical improvement of total optical fiber capacity.

1.1.1.3 Information explosion and short-distance optical interconnects

Recently, given that the information and telecommunications network traffic have been increasing dramatically at a compound annual growth rate (CAGR) of 40% or even more since the beginning of the 21st century as shown in Fig. 1-2 [23], and the overall IP traffic is expected to grow to be almost 132 exabytes per month by 2018 [24]. Specially, global mobile data traffic, majority growth followed by social networks and web browsing such as online video sites and video chat sites [25], has clearly grown at an explosive rate of CAGR of 61% from 2013 to 2018 [26], driven by smart phones and IP enabled services as a real-time entertainment. This expansion of traffic volume is even expected to continue to grow at a CAGR of 92% through 2015 [27] and continue for many years in the future. Consequently, a 1000-fold increase in the current total network capacity will be required.

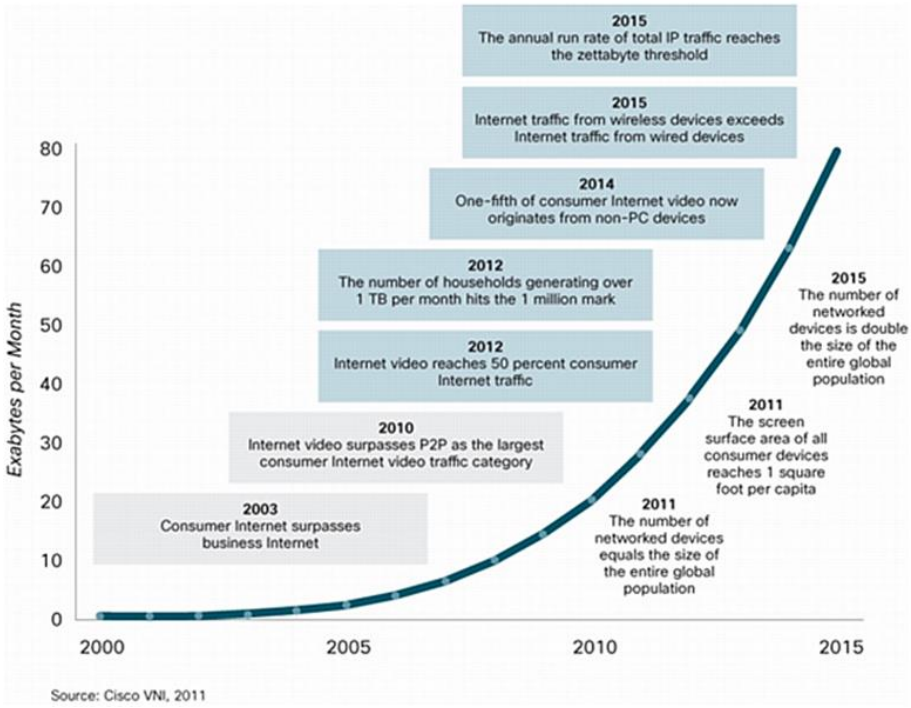


Fig. 1-2 Five traffic milestones and three traffic generator milestones by 2015. [23]

Therefore, the development of optical communication system, employing a combination of WDM and TDM technologies, from the traditional long-haul optical fiber systems to the short-distance interconnects, such as rack-to-rack, board-to-board, and chip-to-chip, even at on-chip level, has been studied intensively and sounds become to be the best opportunity for an ultra-high speed information transmission system.

1.1.2 Photonic integrated circuits to large scale integration

1.1.2.1 The performance bottleneck of large scale integration

The integrated circuits (ICs) technology, which fabricates complex circuits on a silicon semiconductor substrate called wafer, is one of the fundamental technologies supporting the modern computer and digital equipment nowadays. Since 1965 during half a century, according to the Moore's Law [28] and scaling law, the miniaturization technology has been developed significantly and realized a ultra-large scale integration (ULSI) which can integrate 100 million elements. Since 2000, the research of system-on-chip (SOC) has been flourishingly carried out to instead the conventional separate constructions. Simultaneously, process ruler, the minimum size of ICs fabrication described by the gate limit, also has been reduced to 32 nm by the year of 2010, and will be 11 nm in 2022, according to the road map from ITRS [29].

These remarkable growths can be attributed to several technical and economic factors [30]:

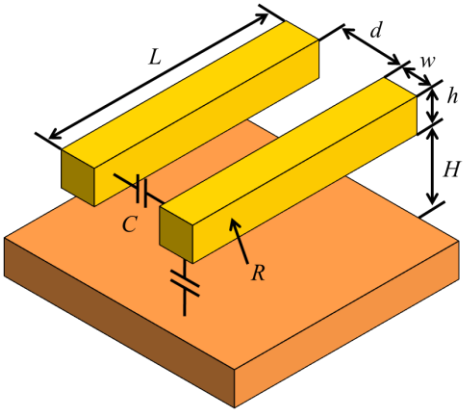
1) the physical design of the planar field effect transistor;
2) ideal compatible materials: single-element silicon substrate, silica insulator, and aluminum wiring;
3) scalable circuit design based on low power complementary metal oxide semiconductor (CMOS) architecture; the cost per transistor drops inversely as the number N of transistors per chip increases;
4) real applications (e.g., memory and microprocessors) that require large-scale arrays of identical elements, which can be scaled down in size, seemingly without limit, as the processing technology advances;
5) progressively complex and successful applications that provide the funds to invest in the processing technology required for the next generation of reduced gate length.

In the meanwhile, some new problems are coming up during proceed of miniaturization.

Firstly, miniaturization leads an increase of total power consumption on chip, as while as the going up of integration. Therefore, after 2005, the CPU clock signal was controlled below 4 - 5 GHz, in order to suppress an increase of power consumption, and parallel arithmetic processing by multicore became common [31].

Secondly, with the miniaturization, a global wiring delay becomes a serious problem. As shown in Fig. 1-3, although the RC delay of local wiring is constant, the length of the global wirings are increasing caused by multicore, and the signal delay among the global wirings become a serious problem. Figure 1-4 (a) shows a cross section view, and (b) shows a relative delay relationship among various wiring sections [29]. Although the miniaturization brings an acceleration of transistor, it is also reported that RC delay in the global wiring and between the LSIs, especially in the case of average wiring length over 10 mm, were greatly influenced [32]. The global wiring signal delay can be controlled in some means by insertion of repeaters, but excessive chip square and power consumption will face new limits.

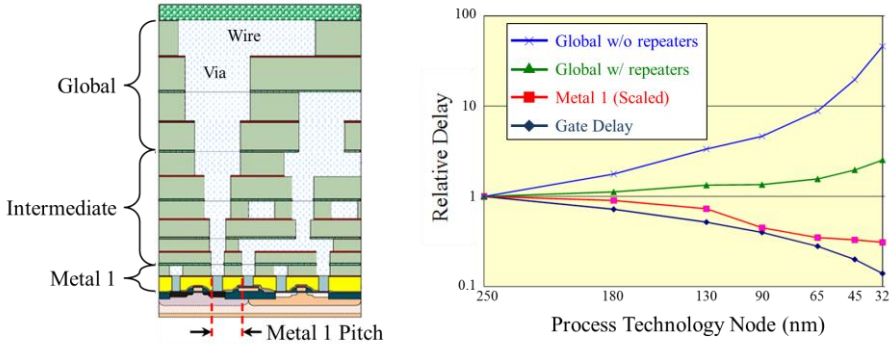
What's more important, although it is possible to reduce wiring spacing in the LSI by miniaturization, the wiring spacing of chip-to-chip is determined by the contact pin spacing between the chip's input-output either printed wiring, which means that it is difficult to catch up the acceleration of processing just utilizing traditional electronic wirings. Therefore, in the last two decades, although the performance of internal wirings has increased 10 thousand times, while the external wirings (chip-to-chip) could not be even 10 times. In addition, due to the wiring length among the chips is much longer than the global wirings, the signal delay become much more serious among chips. In a



Parameters	Local	Global
L	$1/S$	S_C
W, d	$1/S$	$1/S$
H, h	$1/S$	$1/S$
R	S	S^2S_C
C	$1/S$	S_C
T_d $(=RC)$	1	$(SS_C)^2$

S: Device scaling factor
S_C: Chip size scaling factor

Fig. 1-3 The scaling law of LSI.



(a) Typical cross-sectional view of the LSI

(b) Relationship between generation and delay for each layer

Fig. 1-4 A typical cross-sectional view and relative delay of LSI. [61]

conclusion, the increase of signal delay and lack of external wiring volume between LSIs and chips are bottleneck of acceleration and higher-performance systems.

Moreover, the Joule heat, the thermal noise, and the electromagnetic field loss in a high frequency of electric wirings are all inherent problems.

In the long term, new design or technology solutions, such as 3D ICs, free space RF, optical interconnect for the short-distance, will be needed to overcome the delay, power and bandwidth limitations of traditional electric interconnect [29].

Especially, optical interconnects are considered to be the most viable solutions. Figure 1-5 shows a comparison of the relationship between electric and optical wirings by power delay product and wiring length. Given the case of wiring length over 10 mm, it is expected that the performance of optical wiring surpasses that of Cu wiring. Because light has a frequency range around 200 THz, the application of WDM technology can greatly improve the signal bandwidth. Moreover, due to optical wirings are immune to an electromagnetic noise, a cross-talk can be controlled and it is possible to enhance a wiring

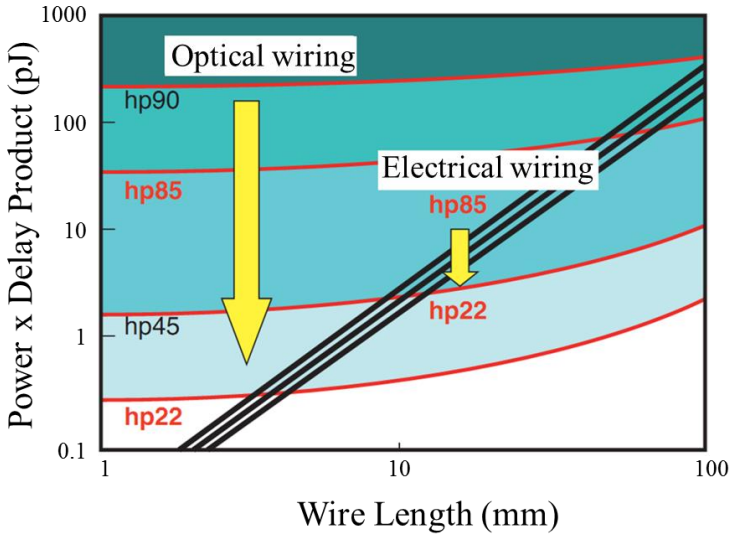


Fig. 1-5 Comparison of the relationship between electric and optical wirings by power delay product and wiring length. [29]

density. Besides, in optical wirings, a cross intersection can be employed, which is impossible in the electric wirings, promising a design freedom [33].

1.1.2.2 Photonic integrated circuits to large scale integration

A photonic integrated circuit (PIC) or optical integrated circuit is a device that integrates multiple photonic functions, like optical lasers, optical amplifiers, optical modulators, multiplexers, de-multiplexers, attenuators, and photodetectors onto one substrate, as such is analogous to an electronic integrated circuit (EIC).

The PIC was first proposed in 1969 [34] and the first commercial application, requiring about 10^2 devices, occurred in about 2005, some 36 years later. The reasons for this lag generally follow the list above in a negative fashion [30]:

1) active photonic device are based on binary, ternary and quaternary materials that are much harder to control than Si;
2) photonic device sizes are determined by the optical wavelength, which is much larger than the electron size limit in EICs;
3) PICs require a wide variety of different devices (e.g., lasers, detectors, modulators, multiplexers, attenuators);
4) few applications that require both large-scale integration and high volume, with attendant low cost, have been identified.

As the capabilities of PICs and EICs advance, it is clear that it would be advantageous to combine to the same substrate both larger-volume PIC functions and high-speed electronic data processing. If the PIC and EIC functions are provided on the same

substrate or chip, we will call this an optoelectronic IC (OEIC).

As in EICs, PICs can include both hybrid and monolithic integration.

In a hybrid PICs, multiple single-function optical devices are assembled into a single package, sometimes with associated EICs, and interconnected to each other by electronic and/or optical couplings. Adding to the packaging challenge is the fact that different materials may require different packaging designs due to differences in optical, mechanical and thermal characteristics, such as different coefficients of expansion, different operating temperatures and thermo-electric coolers, compounding packaging complexity and cost. In practice, these have limited hybrid PICs to integrating at most three to four optical components into a common package.

In contrast, monolithic integration consolidates many devices and/or functions into a single photonic material, so that all photonic couplings occur within the substrate and all functions are consolidated into a single, physically unique device. Monolithic integration provides the greatest simplicity and reliability benefits when consolidating optical components into a single device. This can greatly reduce cost and make transceivers scalable, because the elements are automatically optically aligned to each other and can be tested all at once. It is generally assumed that monolithic PICs perform significantly worse than their discrete-optic counterparts optimized independently, because in an integrated part in which tradeoffs must be made owing to all components are made at once.

1.1.2.3 Comparison of photonic materials and Silicon photonics

Nowadays, optical components are built employing many kinds of materials, each with its respective merits and drawbacks, including element semiconductors (Si and Ge-related), compound semiconductors (InP and GaAs-based), dielectrics (SiO_2 and SiN_x-related), polymers and nonlinear crystal materials (e.g. $LiNbO_3$). The material properties of different material systems place them into desirable, but discrete functionality regimes. There compare the most prominent of them in Table I-1.

Silica-based planar lightwave circuits (PLCs) have provided various important devices for both WDM networks and optical access networks, including power splitters, arrayed waveguide gratings (AWG), thermo-optic switches, and hybrid OEICs in 1990s [35, 36]. Especially, erbium-doped silica had been employed to realize a guided-wave laser operating in a PLCs in 1991 [37]. Moreover, a silica-based PLC is extremely suitable to couple into a optical fiber with an ignorable loss. However, the poor refractive index contrast seriously limits the integration density and volume scaling of PLCs.

Table I-1 Comparison of photonic materials

	Glass	Nitride	Polymer	III-V	Silicon
Integration density	-	+	-	++	+++
Volume scaling		++	++	+	++
Thermal operating budget	+	++	-	+	++
Stability	++	++	-	++	++
Cost	++	+	++	-	+
Lasers	+	-		++	+*
Modulators	-	-	+	++	++
Passives/WDM	++	++	+	++	+
Detectors	-	-	-	++	++
Integrated with electronics	-	-	-	+	+++
Coupling to fiber	+++	+	++	+	+
CMOS compatibility	+	+		-	++

* Implementing lasers in silicon involves heterogeneous integration of III-V materials.

$LiNbO_3$ supplies little promise as a platform material for integration, because it cannot be used to practically implement active opto-electronic devices like lasers and detectors. In addition, complex processing requirements make it not economically useful to large-scale PICs.

To date, InP and GaAs-based materials has been demonstrated the ability to realize an integration of both active and passive optical devices operating in the 1310 nm or 1550 nm telecom-windows with a capability of cost-effective mass production using standard high-yield, batch semiconductor manufacturing processes. Fundamental advancements that have enable PICs technology include the following: the realization and development of semiconductor lasers [38-41], the development of hetero-junction lasers and CW laser operation [42, 43], the realization of quantum-well lasers [44], the development of DFB lasers [45, 46], the development of pseudo-orphic materials (including strained quantum wells) [47-49], and the development of long-wavelength InP-based semiconductor lasers in the low-loss spectrum of the optical fiber [50]. Furthermore, many key advances in technology have enabled the commercialization of PICs, including the availability of high-quality, low-defect density 50 - 100 mm diameter InP substrates, the development of metal-organic chemical vapor deposition (MOCVD) as a viable means for the growth of high-precision lasers and optoelectronics devices [51-53] in multi-wafer reactors, the development of precision dry-etching technologies for low-loss waveguides and highly

reliable devices, and fine line lithography. What's more, the predominantly employed methods consist of one or more combination of butt-joint regrowth [54, 55], selective-area growth [56-59], quantum well disordering/layer intermixing [60-63], and etch-back of multiple vertical device layers [64-68], to enable high-performance operation in different semiconductor layer stacks. In this way, a 40 Gbps InP-based single-chip all-photonic transceiver has been demonstrated in a university lab recently [69]. InP chip maker *Infinera* launched 10-channel and 40-channel 10 Gbps channel transmitters and receivers for DWDM data communication at an aggregate rate of 400 Gbps followed by 40-channel InP transmitters at an aggregate rate of 1.6 Tbps [70].

Silicon photonics

The primary advantages of the Si material system are the abundance of Si, Si makes up 27% of the mass of the Earth's crust, and its companions O and N are also plentiful. The high mechanical strength of Si allows for large wafers, the industry currently focusing on from 300-mm-diameter to 400-mm-diameter for EICs. Si's high-quality oxide SiO_2 has extremely low optical loss and is an excellent electrical insulator. For instance, a very small core waveguides of silicon nitride (Si_3N_4) embedded in SiO_2 on a Si wafer, in which most of the light resides in the oxide cladding, achieved a waveguide loss of 0.03 dB/cm [71]. On the Si substrate there can be SiO_2, Si_3N_4, SiON (Silicon oxynitride) [72], Ge and various metal such as Al, Cu, and W. For the Si, there can be crystalline Si (c-Si), amorphous Si (a-Si), and polycrystalline Si (p-Si) [73-76]. The distinction between a-Si and p-Si is blurry, p-Si having larger single-crystal domain, a-Si can be converted to p-Si by annealing.

Since the optical absorption of single c-Si becomes negligible at a wavelength longer than 1.1 μm, an extremely low propagation loss of 0.35 dB/cm, which is better than the value reported for optical waveguides consisting of III-V materials [77]. Therefore, recently, enormous effort has been devoted to realize functional photonic devices/integrated circuits on Si or Si-on-insulator (SOI) substrates by means of advanced Si-CMOS technologies [78-80], and a new field called "Silicon photonics" is being established [81].

Passive optical components and functional photonic integrated circuits exhibiting extremely low scattering loss have also been reported, i.e., considerably low 90° bending loss of 0.01 dB with a 2 μm radius [82] and an extremely high Q factor exceeding 1000 000 with a 2-D photonic crystal resonator [83] were achieved using a SOI substrate with a Si layer of 200–300 nm thickness. Si has shown promise as a materials platform for the large-scale integration of passive optical devices, such as optical buffers [84], and switches [85] and AWGs, optical switches and VOAs [86]. In addition, silicon photonic

integrated circuits can be built using standard CMOS processes and therefore hold promise for enabling both optical and electronic integration.

In the case of light sources based on Si or SOI substrates, the CW operation of a Raman silicon laser was demonstrated under optical pumping [87]. Furthermore, a moderately low power consumption of 20 mW, as well as a high differential quantum efficiency of 28% was achieved [88]. A direct gap transition from Ge-on-Si was also reported [89] and its CW operation under optical pumping was demonstrated at room temperature [90]. The RT-CW operation of injection-type III–V semiconductor lasers on Si substrates prepared by means of epitaxial growth and a wafer direct bonding method [91-94] were reported in the 1980s and 1990s at a wavelength of 1.3 μm [95] and 1.55 μm [96].

Recently, long wavelength lasers grown on Si substrates were developed using GaSb [97] and Ga(NAsP) [98] compound semiconductors. Long wavelength injection lasers have also been prepared by benzocyclobutene (BCB) polymer bonding [99] and low temperature oxygen plasma-assisted bonding [100]. For the functional operation as well as the monolithic integration of these lasers on SOI waveguides, facet-free lasers evanescently coupled with Si waveguides were proposed [101-103]. Whereas most of these lasers have similar threshold currents and light output characteristics as conventional double-hetero-structure lasers, an extremely low threshold current of less than 100 μA was achieved with vertical-cavity surface-emitting lasers (VCSELs) [104] and micro-disk lasers [105]. The latter are characterized by the very small volume of the active region as well as high reflectivity mirrors (high Q cavities). Recently, BCB-bonded micro-disk lasers were reported and a thresh current as low as 0.35 mA was achieved [106-108]. A 2-D PC laser with a thin slab waveguide structure is another promising candidate for on-chip optical wiring. In particular, a threshold current of 0.23 mA can be achieved with a single cell PC laser [109]. An extremely low threshold operation and a fairly high differential quantum efficiency was reported under optical pumping for a 2-D PC-based short cavity laser with a thin (150 nm) slab waveguide structure emitting at 1.55 μm wavelength [110]. Finally, low pulse energy of 8.8 fJ/bit was achieved with a 20 Gbit/s nonreturn-to-zero (NRZ) signal [111].

Recently, high-speed optical detectors as well as electro-optic modulators based on SOI substrates have been reported. Specifically, Ge detectors with such high speed as 30 GHz were achieved using SOI substrates [112–116]. As for modulators based on Si, a Mach-Zehnder interferometric modulator with a 3-dB cutoff frequency higher than 30 GHz [117], a four-channel wavelength division multiplexed microring modulator with a speed of 50 Gbit/s [118], a CMOS modulator with an optical pulse energy of 400 fJ/bit under a driving voltage of 1 V [119], and many more have been reported.

In a word, silicon photonics, with its high index contrast coupled to state-of-the-art silicon process technology can be used to integrate almost all building blocks necessary to construct WDM links on a chip, realizing very dense circuitry and more complex functionality. However, the large sensitivity to fabrication variation and operational conditions, especially temperature, are significant challenges to implement all-silicon optical interconnect.

1.1.2.4 850 nm VCSELs

The concept of the vertical-cavity surface-emitting laser (VCSEL) was proposed in 1977 by *Iga* at the Tokyo Institute of Technology [104]. The reason for the explosive development of VCSELs is their simpler packaging design, smaller size, fabrication of 2D arrays and integration, on wafer testing, and manufacturability. The particular combination of band gap and refractive index differences in GaAs, AlAs, and alloys of AlGaAs, as well as the incredible level of control that was developed for both molecular beam epitaxy (MBE) and metalorganic vapor phase epitaxy (MOVPE), enables highly reproducible manufacture of device structures. Especially, the small volume of the resonator and the active region enable low-threshold current and efficient high-speed modulation at low currents. Properly designed VCSELs are able to operate over a wide range of temperatures with minimal change in performance.

Therefore, data communication was the first considerable driver for the development of the VCSEL technology [120], and led to significant improvements of VCSEL performance in terms of efficiency, speed, and reliability. VCSELs are now well established as cost-effective and power-efficient optical sources in transmitters for short-distance, high-capacity optical interconnect. A great deal of effort has consequently been undertaken to improve the high-speed performance of VCSELs. The modulation speed of a VCSEL is limited by the intrinsic damping of the resonant carrier-photon interaction, and by effects of self-heating and electrical parasitic. To reach high modulation bandwidths and bit rates, efforts were primarily focused on maximizing the resonance frequency through improved differential gain ($\partial g/\partial n$) [121], minimizing the electrical parasitic [122], minimizing self-heating [123], and optimizing the photon lifetime [124].

Recently, 850 nm VCSELs with a 3 dB bandwidth of 23 GHz at room temperature and 40 Gbps error-free transmission were reported by Chalmers University [125]. In addition, *Finisar* has also demonstrated an 850 nm VCSEL with a 24 GHz modulation bandwidth at room temperature and 15 GHz at 95 °C, which is the highest bandwidth ever reported for 850 nm datacom VCSELs. The high bandwidth of the *Finisar* VCSEL was achieved

by maximizing the differential gain rather than by reducing the photo lifetime. Furthermore, error-free transmission at bit rates exceeding 40 Gb/s using VCSELs emitting at 850 nm, 980 nm, and 1.1 μm was reported by multiple groups [126-128]. A VCSEL-based link operating error-free at a record-high speed of 56 Gbps was recently demonstrated by *Finisar* and *IBM* [129].

1.1.2.5 The innovation of active optical cable and Si-CMOS photonics

Nowadays, information traffic from data centers are now a major driving force behind the Internet, and the largest data centers are orders of magnitude larger than the supercomputing centers. In order to realize an ultra-high and large-volume short-distance optical interconnects in the data centers, an active optical cable (AOC) technology has attracted much attention from both research institutions and industry. An AOC is a cabling solution that mates to the same electrical ports as a traditional copper cable, but uses optical fiber in place of copper conductors. In order to improve the cable's distance and speed performance without sacrificing its compatibility with standard electrical interfaces, the AOC uses electrical to optical conversion on the cable ends.

The AOCs market is largely driven by the rise in the processor speeds, growing demand for higher bandwidth speeds, especially new consumer bandwidth demands up to 20 Gbps. Until quite recently, AOCs have continued to be deployed to optimize the existing infrastructure by providing higher data rates among servers, switches and storage facilities within the data centers. Overall the AOC's market reached approximately $40 million in 2010 with unit shipments of 150,000, and it will hit $0.7 billion by 2018, while data centers will contribute $0.5 billion. [130, 131].

Given the practical application of silicon optical short-distance interconnects, Si-CMOS photonics continues to move into mainstream market sectors by enabling flexibility, scalability and throughput, for truly universal optical connectivity in low-cost bandwidth. Recently, in the front-end chip manufacturers, such as Intel and IBM, everyone put Si-CMOS photonics as major research and development.

Luxtera, an industrial leader in CMOS photonics, announced a 40 Gbps optoelectronic transceiver in a quad small form factor pluggable (QSFP) module in 2013, containing a 4 channels x 10 Gbps, 0.13 μm CMOS SOI integrated optoelectronic transceiver chip co-packaged with a semiconductor laser, which is the only component not fabricated in a CMOS production line and flip-chip bonded onto a CMOS chip later on [132].

In 2009 December, *Intel* showed the experimental study of 48 core processor (Single-chip Cloud Computer), its performance is 10 ~ 20 times more than the series of

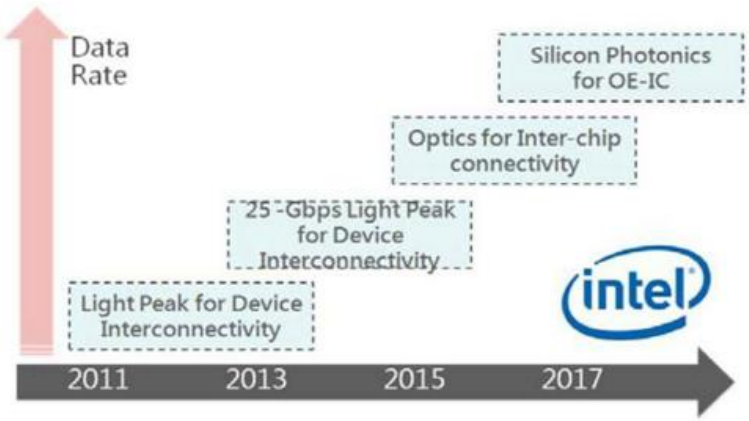


Fig. 1-6 The predictive process development of optical technology by *Intel*. [133]

Intel Core. *Intel* estimated the process of optical technology development as shown in Fig. 1-6, Bard to Board optical technologies reached 10 Gbps for each channel in 2011, that is 2 channels x 10 Gbps for Light Peak module technology. Chip on chip technologies have an opportunity to reach 25 Gbps for each channel in 2015. Intra-chip interconnect is scheduled to be used practically in 2020 [133].

In 2010 December, at Semicon Japan, *IBM* predicted that "Silicon Nano-Photonic" would be a key to achieve "exascale" processor in the future, it could reach a million trillion operations per second. By using the light (electrical-to-optical, and optical-to-electrical) transceiver integrated into traditional CMOS chip, as shown in Fig. 1-7, this silicon photonic technology is positively evaluated to breakthroughs the bottleneck of currently developed on exascale computing platform [134].

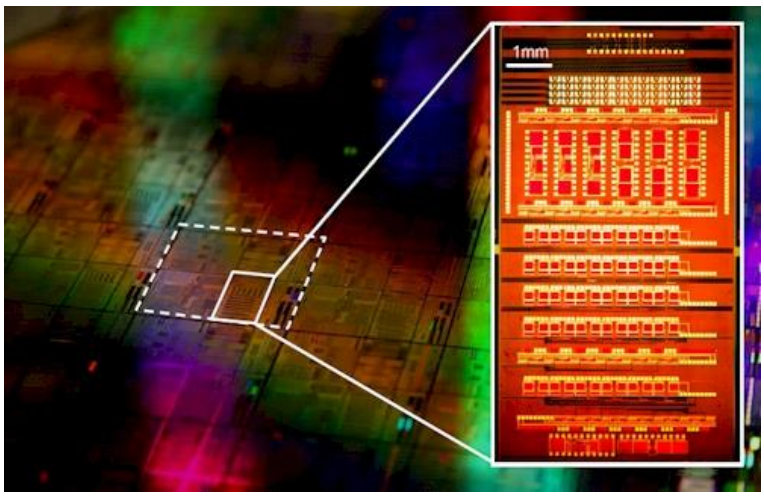


Fig. 1-7 *IBM*'s nanophotonics components: integration of the ring oscillator, receiver amplifier, transmitter modulator driver, waveguides, edge fiber coupler, wavelength division multiplexer, germanium detector, modulators, and switches on one CMOS chip. [134]

1.2 Objectives

As the capabilities of PICs and EICs advances, it is clear that it would be advantageous to combine on the same substrate both PICs functions and high-speed electronic data processing.

The use of PICs fundamentally changes the economic threshold for implementing ubiquitous OEO conversion across an optical network. This enables the design of a new architecture, a digital optical network (DON) that combines the traffic management flexibility and engineering simplicity of digital transport systems with the bandwidth scalability of WDM and the affordability of large-scale photonic integration [135].

Therefore, this study was carried out to realize an AOC integrated with Si-LSIs, as shown in Fig. 1-8. Especially, given an integrated circuit of a large-volume optical interface to a high-performance electrical LSI processing is proposed to lead a generational communication system. In order to enable a cost-effective implementation of thus optical short-distance connections, a CMOS compatible process is an useful, low-cost approach for a monolithic integration of available, complex, and high-speed optical circuits, combining with general 850 nm transmitters and platform Si photodetectors to form an OEIC on a Si substrate.

In this wavelength range, a relatively high refractive index material SiN_x [136], or an ultra-high refractive index amorphous material, amorphous silicon (a-Si) [137], or some high-κ and ferroelectric materials, such as Ta_2O_5, Nb_2O_5, TiO_2, Zn_2O, CeO_2, can be candidates of an optical waveguide material.

Low loss Si_3N_4 waveguide has been reported by numerous researchers. In the case of a-Si, although depending on the condition of deposition process, the band gap has a value in a range of 1.4~1.8 eV, means it can transmit light in 850nm wavelength range.

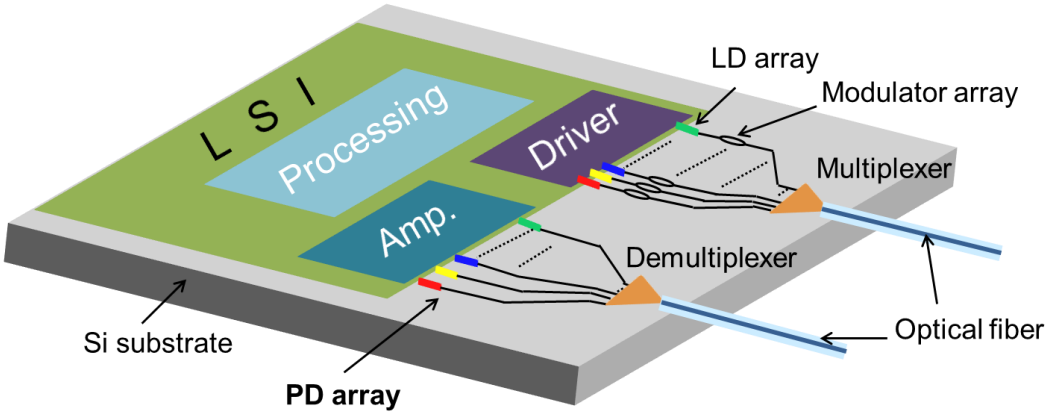


Fig. 1-8 A schematic structure of AOC integrated with Si-LSIs.

Moreover, owing to an ultra-high refractive index of a-Si about 3.7 in this wavelength range, a strong light confinement can be obtained. Furthermore, using a Chemical Vapor Deposition (CVD) method, a-Si or a-Si:H can be deposited at a low temperature, showing a possible consistency with the CMOS process [138]. There were also some reports that low loss a-Si optical waveguides were achieved in 1310 nm or 1550 nm wavelength range [139, 140].

A schematic structure of the optical integrated circuit of waveguide and photodetector is shown in Fig. 1-9. A low-loss high-refractive-index tantalum pentoxide (Ta_2O_5) waveguide and an ultra-high speed Si-PIN photodetector (Si-PIN PD), utilizing a directional waveguide grating coupler in the 0.8 μm wavelength range.

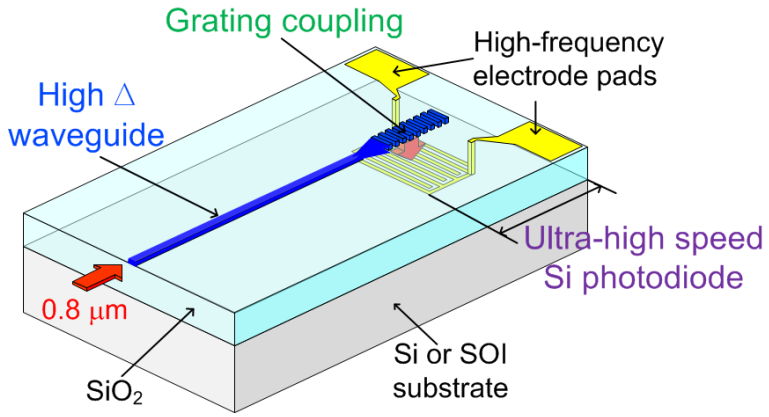


Fig. 1-9 The schematic structure of waveguide and photodetector integrated circuit.

1.3 Organization of this dissertation

In this chapter of introduction, a historical review of the innovations and developments from long-haul optical fiber communication technology to short-distance optical interconnects is discussed at first. And then, as the background of this study, some theoretical discussions and technology issues were argued for realizing an AOC integrated with Si-LSIs.

In chapter 2, a high-refractive-index (n ~2.0) and low propagation loss (< 1 dB/cm) Ta_2O_5 waveguide was realized. A Ta_2O_5 strip optical waveguides with a cross section of 400 nm x 10 μm was fabricated by a chemical solution deposition followed by a CF_4 reactive ion dry etching. The optimum fabrication steps make it possible to obtain the Ta_2O_5 strip optical waveguides with a propagation loss of less than 1 dB/cm at 830 nm, which is significant for OEICs in the 0.8 μm wavelength range.

In chapter 3, a directional waveguide grating coupler was calculated by using finite element method (FEM) to achieve a bottom directional coupling efficiency > 60% with a grating length of 15 μm, at a grating period of 530 nm, a duty ratio of 0.5, and an etching depth ratio > 0.9 with a thickness of 400 nm.

In chapter 4, a design and implementation of lateral Si-PIN PDs fabricated on an SOI substrate (absorber layer thickness of 210 nm) in the CMOS compatible process is reported. In addtion, we disscussed structure dependences on the frequency and optimum design for a maximum bandwidth. A standard device fabricated with a finger width of 1.00 μm, a finger spacing of 1.63 μm, a square detector area of 20 × 20 μm^2, and a pad size of 60 × 60 μm^2 achieved a bandwidth of 12.6 GHz at a bias voltage of 10 V, with a responsivity of 7.5 mA/W at 850 nm wavelength. Photodetector with the same geometry, which was fabricated with a smaller pad size of 30 × 30 μm^2 exhibited a bandwidth of 13.6 GHz.

In chapter 5, there will be a brief summary of this study and give some future works on this study.

Chapter 2

High Refractive Index Contrast Optical Waveguide

2.1 Organization of this chapter

In this chapter, firstly I will discuss some basic characteristics of waveguide for optical integrated circuits by using waveguide parameters of refractive index contrast (Δ) and normalized frequency (V). Given Δ dependences of bending radius, phase error, polarization dependence, and fabrication tolerance, I proposed a waveguide material, tantalum pentoxide (Ta_2O_5), with the $\Delta \sim 20\%$, which can realize a bending radius less than 10 μm (< 0.1 dB/90°) and not much serious fabrication tolerance (10 nm order), simultaneously.

Then, I will descript the deposition of a Ta_2O_5 thin film and the fabrication of Ta_2O_5 strip optical waveguides on a silica substrate, and the measurement of propagation loss was carried out in the 0.8 μm wavelength range, particularly.

2.2 Introduction

2.2.1 Characteristics of waveguide for optical integrated circuits

Optical waveguide, as an optical signal channel among sorts of optical devices, is one of the most fundamental components in the optical interconnection. Propagation loss and size can be evalutated as the basic capabilities of a waveguide. The propagation loss depends on: (1) an absorption loss, means a carrier absorption in the material, has a wavelength dependence on usual; (2) a scattering loss, which means radiation to the substrate or cladding layer from the interfaces or sidewalls of waveguide, is mainly dependent on the fabrication and Δ. The absorption loss is dominant in a doped waveguide, and scattering loss is large influential while the cross section of the waveguide become relatively smaller. As so far, it has been reported that waveguides made of silica and polymer have low loss below 0.1 dB/cm. However, because of the low refractive index (n) and low Δ, light confinement is relatively weak. As a result, it is necessary to increase the bending radius, the spacing among the waveguides to avoid cross talking, and accept a large cross section.

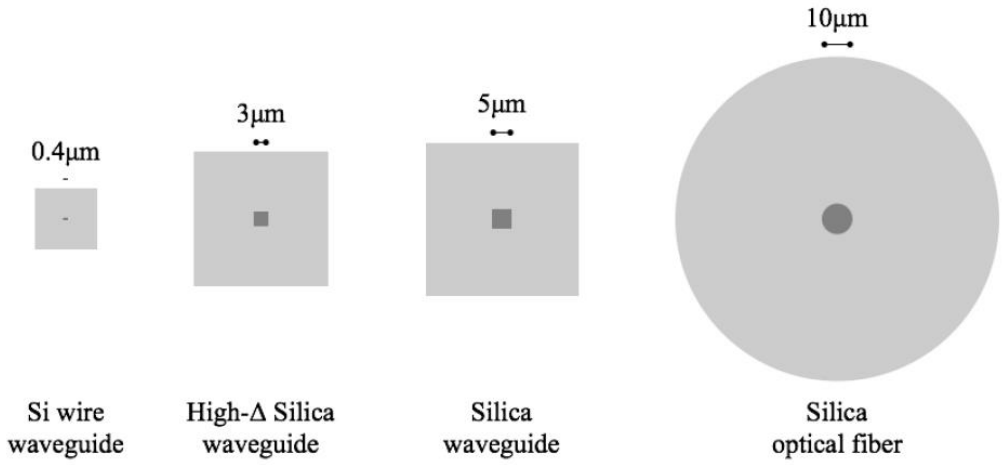


Fig. 2-1 A schematic view of various optical waveguides and optical fiber.

For example, a silica waveguide Δ is about 0.5%, and over 1 cm bend radius is required for a low bending loss. It is unfavorite in a high density PICs, and difficult to realize the connection between optical wirings on a LSI. Therefore, in recent years, a silicon photonics apply a thin wire waveguide utilizing Si (n ~ 3.5) as a core cladding with SiO_2 (n ~ 1.44) [141]. Because of the ultra-high Δ ~ 40% of the Si thin wire waveguide, the optical filed is confined strongly in the core. A low 0.01 dB/90° bending loss in a 2 μm bend radius, with a waveguide cross section of 200 nm x 400 nm has been reported [142]. Figure 2-1 shows a schematic view of various optical waveguide and optical fiber in proportion.

However, the utilization of a ultra-high Δ waveguide, such as Si wire waveguide, will also bring many drawbacks, such as an increase of propagation loss, a large coulping loss to the fiber, a degradation of cross talk in the interference components, polarization dependences of center wavelength and loss, destabilization of center wavelength, polarization cross talk, and reflection in the boundary surface. It is necessary to solve these fundamental issues, in order to employ a high Δ waveguide.

In the following, I will review some fundamental charateristics according to the Δ of optical waveguide, and give some ideas to overcome the problems of high Δ optical waveguide.

2.2.2 High refractive index contrast (Δ) optical waveguide

2.2.2.1 Parameters of optical waveguide

In the analysis of 2-dimensional slab waveguide, it is possible to describe the basic properties of the waveguide by the standardized parameters. For the 3-dimensional optical waveguide, a numerical analysis approach must be employed, in order to seek the exact solution, but maybe a poor outlook. Therefore, we apply the equivalent refraction method to forecast the characteristic.

We define the refractive index contrast Δ, and the normalized frequency V, as two fundamental parameters as follow:

$$\Delta \equiv \frac{n_f^2 - n_c^2}{2n_f^2} \cong \frac{n_f - n_c}{n_f} \text{ (weak-guidance approximation)} \quad (2.1)$$

$$\mathrm{V} \equiv k_0 a \sqrt{n_f^2 - n_c^2} = k_0 a n_f \sqrt{2\Delta} = k_0 a n_c \frac{\sqrt{2\Delta}}{\sqrt{1-2\Delta}} \quad (2.2)$$

where, n_f is the refractive index of core, n_c is the refractive index of cladding layer, k_0 is the wave number of free space, and $d = 2a$ is the waveguide full-width.

Firstly, a refractive index contrast (Δ) is shown in Fig. 2-2, as a cladding of SiO_2 (n=1.45) is assumed. The optical fibers are almost $\Delta \approx 0.3\%$, and a traditional PLC employing a silica or polymer core has a $\Delta \approx 0.3 \sim 1.5\%$. Against, the silicon waveguide has an ultra-high Δ more than 40%.

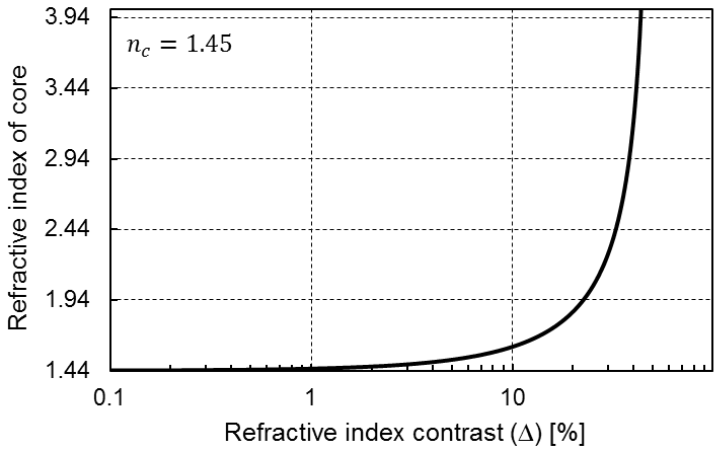


Fig. 2-2 A refractive index contrast Δ as a cladding of SiO2 (n=1.45).

It can be derived from Equ. (2.2) that a waveguide width is proportional to the $\Delta^{-0.5}$.

$$d = 2a = \frac{2V}{k_0 n_c}\sqrt{\frac{1-2\Delta}{2\Delta}} = \frac{\lambda}{2n_c}\sqrt{(2\Delta)^{-1} - 1} \propto \Delta^{-0.5} \quad (2.3)$$

In Fig. 2-3, when $V = \pi/2$, the cut-off condition of higher-order mode, it shows a Δ dependence of the single-mode waveguide width. As a higher Δ, it can be predicted that the core width becomes smaller than μm size. Especially, when the $\Delta > 30\%$, the core with is decreasing rapidly to realize a miniaturization, but as the same time, an extreme miniaturization processing is necessary.

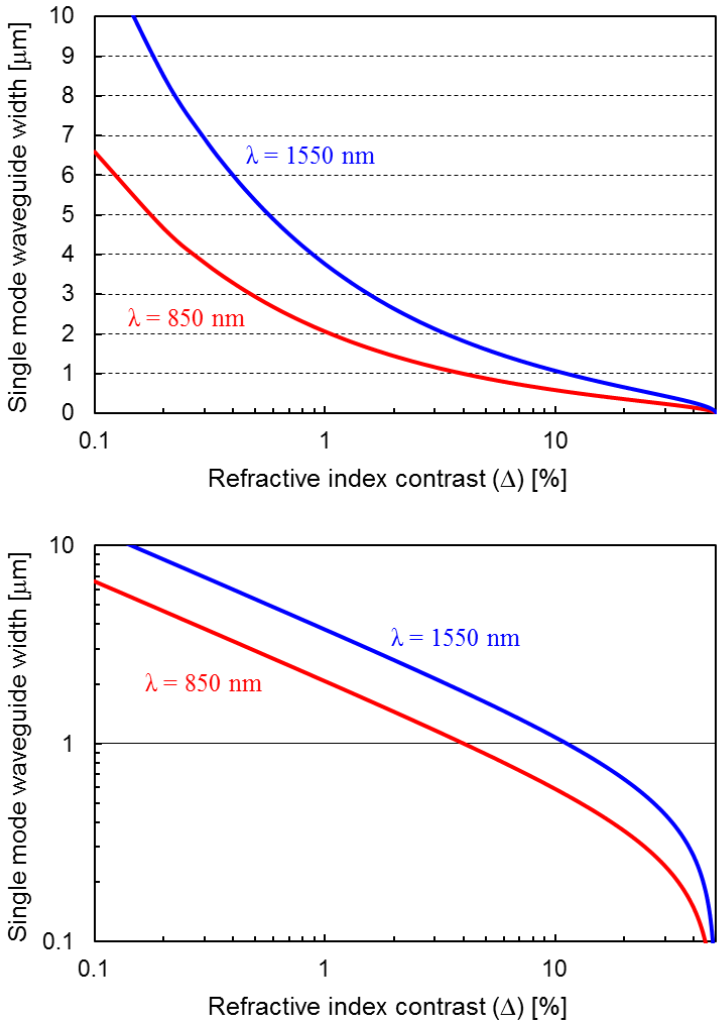


Fig. 2-3 Δ dependence of single mode waveguide width at λ = 850 and 1550 nm.

2.2.2.2 Bending radius of optical waveguide

It is useful to apply a conformal transformation method to analysis curved waveguides by *Heiblum* and *Harris* [143]. By changing the coordinate, a curved waveguide with a certain bend radius can be regarded as a straight waveguide with a certain refractive index gradient, shown in Fig. 2-4.

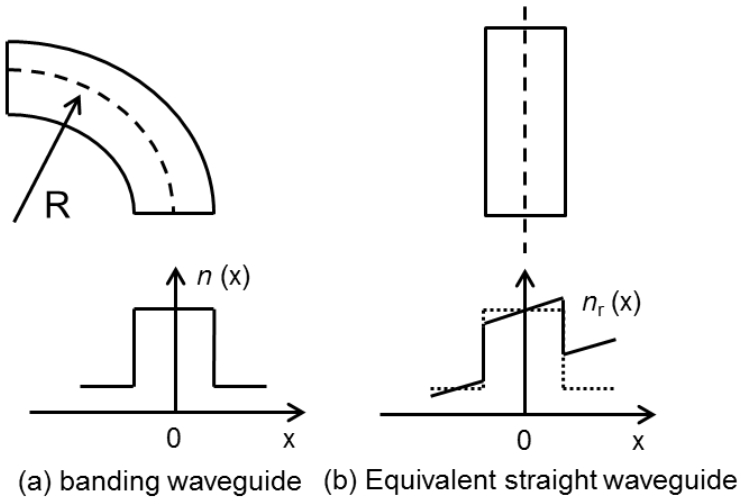


Fig. 2-4 Banding waveguide and equivalent straight waveguide.

Here, $n_r(x) = n(x) \cdot (1 + \frac{x}{R})$, with a certain bend radius R. Then, we can find a transition point, where the propagation constant β is equal c, means the boundary of a propagation mode. For this reason, there will exist a minimum bending radius for the confinement mode, and only leakage mode existing over the boundary condition. From a theoretical analysis by *Marcuse* [144], a radiation power loss coefficient for the dominant mode of the bent step-index slab waveguide can be written as follow,

$$\alpha_B = \frac{k^2\gamma^2 e^{2\gamma a}}{\beta(1+\gamma a)(k^2+\gamma^2)} \exp(-\frac{2\gamma^3}{3\beta^2}R) \tag{2.4}$$

Given a slab waveguide is bent into a circle with radius R. The parameter n_f is the refractive index of core, n_c is the refractive index of cladding layer, k_0 is the wave number of free space, and $d = 2a$ is the waveguide full-width. k is related to the propagation constant β, as $k = \sqrt{n_f^2 k_0^2 - \beta^2}$, and γ is defined as $\gamma = \sqrt{\beta^2 - n_c^2 k_0^2}$. In addition, from the Maxwell's equations in isotropic and lossless dielectric material, given $U = ka, W = \gamma a$, the eigenvalue equation can be written as follow:

$$V^2 = W^2 + U^2 \tag{2.5}$$

$$W = Utan(U) \text{ (TE mode)} \quad W = \left(\frac{n_f}{n_c}\right)^2 Utan(U) \text{ (TM mode)} \tag{2.6}$$

Here, given $\Delta < 1/2$, and

$$\beta \approx k_0 n_f = \frac{V}{a\sqrt{2\Delta}} \tag{2.7}$$

α_B can be rewritten into

$$\alpha_B = \frac{U^2W^2e^{2W}2\Delta(k_0n_f)}{(1+W)V^4}\exp(-\frac{2W^3k_0n_f(2\Delta)^{1.5}}{3V^3}R) \quad (2.8)$$

Then, by multiplying the propagation distance $R\theta$, a propagation loss α_θ can be written as follow:

$$\alpha_\theta = R\theta\frac{U^2W^2e^{2W}2\Delta(k_0n_f)}{(1+W)V^4}\exp(-\frac{2W^3k_0n_f(2\Delta)^{1.5}}{3V^3}R) \quad (2.9)$$

Here, as a bending radius $x = 1/R$, in the domain of $x \fallingdotseq 0$ with the approximation $x \cong exp(ax^{-0.1})$, it can be derived that the minimum bending radius is proportional to $\Delta^{1.6}$. In common, given a regulation that a bending loss less than 0.1 dB/90°, here show the result of Δ dependence of the minimum bending radius regarding an embedded waveguide in Fig 2-5. A few percent or higher Δ is necessary to realize a bending radius around 100 μm. Especially, a 10 μm extent bending radius, which is necessary to realize PICs with or on LSI, expect a Δ about or higher than 20%.

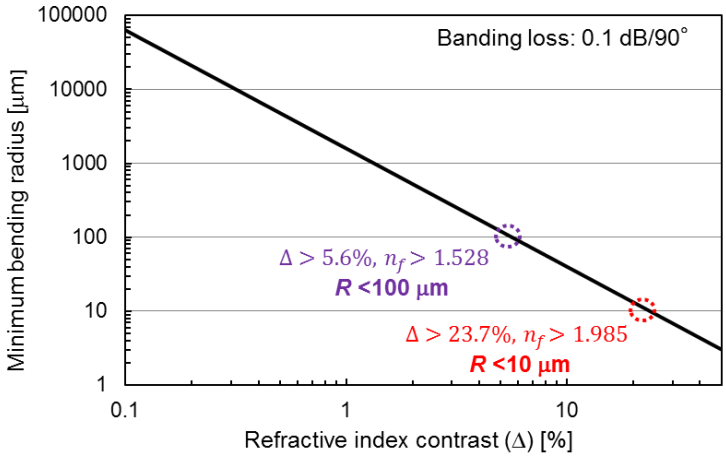


Fig. 2-5 Δ dependence of minimum bending radius at banding loss < 0.1 dB/90°.

2.2.2.3 Scattering loss of optical waveguide

It is well known that some slight structural incompletion in the boundary surface of waveguide will affect the propagating light and lead a scattering wave. According to some theoretical analysis by *Marcuse*[145], *Suematu* [146], and *Haus* [147], especially, the report by *Lacey* and *Payne* [148, 149] is regarded as the most elegant analysis methods to analyze a high Δ waveguide. Propagation loss α can be represented as an exponential autocorrelation relationship of the surface roughness function $R(u) = \sigma^2 \cdot \exp(-|u|/L)$.

$$\alpha = \varphi^2(a)\left(n_f^2 - n_c^2\right)^2\frac{k_0^3}{4\pi n_f} \times \int_0^\pi \frac{2\sigma^2L}{1+L^2(\beta-n_ck_0cos\theta)^2}d\theta \quad (2.10)$$

Where, σ^2 is an average value of the square of the surface roughness, L is the correlation length. Then the electric field intensity in the waveguide boundary surface $\varphi^2(a)$ can be written as follow, where P_g is the power of propagation light.

$$\varphi^2(a) = \frac{\cos(U)^2}{P_g} = \frac{U^2}{V^2} \cdot \frac{W}{1+W} \cdot \frac{2}{n_f} \sqrt{\frac{\mu_0}{\varepsilon_0}} \frac{1}{a} \tag{2.11}$$

$$\alpha = \frac{U^2}{V^3} \cdot \frac{W}{1+W} \sqrt{\frac{\mu_0}{\varepsilon_0}} \left(\sqrt{2\Delta}\right)^5 \frac{k_0^4 n_f^3}{2\pi} \times \int_0^{\pi} \frac{2\sigma^2 L}{1+L^2(\beta - n_c k_0 cos\theta)^2} d\theta \propto \frac{\Delta^{2.5} n_f^3}{\lambda^4} \sigma^2 \tag{2.12}$$

According to a normalized function by *Ladouceur* [150], α can be rewritten as

$$\alpha = \frac{1}{a^5 \beta} \cdot \frac{V^2 U^2 W}{1+W} \cdot \int_0^{\pi} S(\beta - k n_c cos\theta) d\theta \tag{2.13}$$

Given the correlation length L is sufficiently larger than waveguide width $2a$, and the integral term in the Equ. (2.10) to (2.13) can be considered independent on Δ. In the case of a same V, the waveguide scattering loss can be approximate proportional to the $\Delta^{2.5}$, and the square of surface roughness. Figure 2-6 shows the Δ dependence of scattering loss with the same V and roughness in normalized at Δ= 1%. With an increase of Δ, the scattering loss will increase rapidly. Consequently, in order to realize a low loss waveguide with high Δ, an extremely micro-fabrication technology is necessary to suppress the unevenness in the sidewall of waveguide. On the other hand, there is another method to reduce the scattering loss without decreasing surface roughness. From Equ. (2.12), the scattering loss is inversely proportional to V^3, what means scattering loss can be reduced by employing a higher V waveguide.

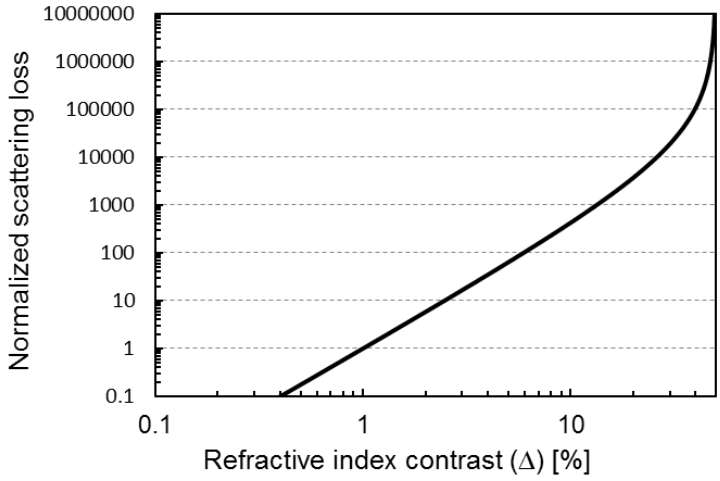


Fig. 2-6 Δ dependence of normalized scattering loss.

2.2.2.4 Phase error of optical waveguide

In the interference devices, such as AWG, a phase error of waveguide is an important parameter to decide the components dispersion and crosstalk characteristic. The reason of the phase error is attributed to many factors, such as the non-uniformity of waveguide fabrication dimension, deposition thickness and refractive index. Especially, even a high Δ waveguide could suppress the deposition non-uniformity owing to a smaller size and thin thickness, the non-uniformity of waveguide width processing has become more influence than other factors.

Considering the non-uniformity influence in the waveguide width processing, there exists an average value of pattern dimension variation, Δa, which can be given as a constant without depending on Δ in a same fabricating technology. The phase error can be represented as a phase variation regarding to the average pattern dimension change, $\Delta\Phi \propto \frac{dn_{eq}}{da}$.

If we define the normalized propagation constant b as follow,

$$b = \frac{n_{eq}^2 - n_c^2}{n_f^2 - n_c^2} = \left(\frac{W}{U}\right)^2 \tag{2.14}$$

The slope of the effective refractive index, dn_{eq}, with the waveguide width variation can be written as follow:

$$\frac{dn_{eq}}{da} = \frac{n_f^2 \Delta}{2n_{eq}} \cdot \frac{db}{dV} \cdot \frac{dV}{da} = \frac{n_f^3 (2\Delta)^{1.5} \pi}{n_{eq} \lambda} \cdot \frac{db}{dV} \propto n_f^2 \Delta^{1.5} \frac{db}{dV} \tag{2.15}$$

Regard with the same variation of pattern dimension Δa, the change of n_{eq} is proportional to $\Delta^{1.5}$. Given the n_{eq} and the center wavelength of wavelength division multiplexer have a linearly proportional relationship, therefore a variability of the center

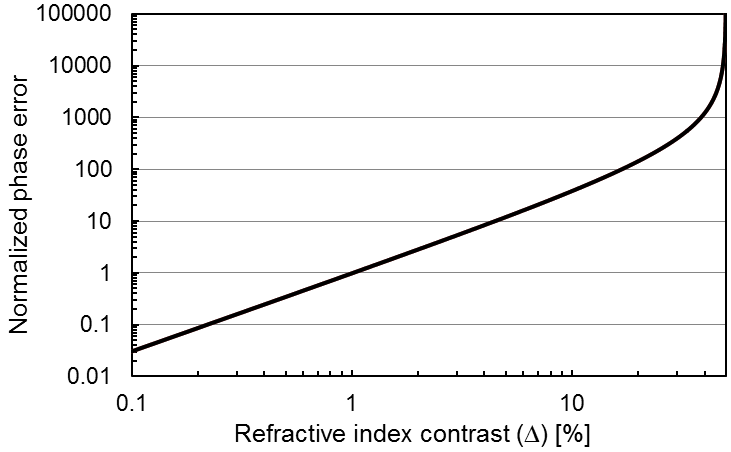


Fig. 2-7 Δ dependence of normalized phase error.

wavelength is proportional to $\Delta^{1.5}$. Figure 2-7 shows the Δ dependence of phase error in normalized at $\Delta = 1\%$.

The phase error will lead to a degradation of crosstalk characteristic in high Δ waveguide AWG. For example, making 10 times larger of the Δ will increase 32 times of phase error and 30 dB degradation of crosstalk. This significant degradation in crosstalk appears to be a serious problem in the application of wavelength division multiplexer. This is maybe a background of the fact that an AWG made of Si thin wire waveguides is unable to acquire favorable characteristic, even in spite of an advanced fabrication process [151].

2.2.2.5 Polarization dependence and fabrication tolerance of optical waveguide

Even utilizing a waveguide design of polarization independent, optical waveguides have birefringence resulted from fabrication error of waveguide width. The center wavelength of WDM and wavelength filter is also determined by the difference of birefringence, so it is crucial to decrease the birefringence. In the following, according to the boundary condition of a slab waveguide, we can seek an approximation of the Δ dependence of polarization independent tolerance, regarding to variation of waveguide width.

Firstly, given the case of a square channel waveguide, as a polarization independent condition of TE and TM, we assume $W_{\mathrm{TE}} = W_{TM}, U_{TE} = U_{TM}$ are established.

$$\frac{db}{dV} = \frac{2W}{V^2}\left(\frac{dW}{dV} - \frac{W}{V}\right) \tag{2.16}$$

$$\frac{db}{dV}_{TE-TM} = \frac{2W_{TE}}{V^2}\left(\left(\frac{dW}{dV}\right)_{TE} - \frac{W_{TE}}{V}\right) - \frac{2W_{TM}}{V^2}\left(\left(\frac{dW}{dV}\right)_{TM} - \frac{W_{TM}}{V}\right)$$

$$= \frac{2W_{TE}}{V^2}\left(\left(\frac{dW}{dV}\right)_{TE} - \left(\frac{dW}{dV}\right)_{TM}\right) = \frac{2W}{V^2}\left(\frac{dW}{dV}\right)_{TE}\left(\frac{n_c^2 - n_f^2}{n_c^2}\right) \propto \Delta \tag{2.17}$$

From Equ. (2.15), the variation of birefringence regarding to the fabrication tolerance of waveguide width can represented as follow:

$$\left(\frac{dn_{eq}}{da}\right)_{TE-TM} = \frac{n_f^5 (2\Delta)^{2.5}\pi}{n_c^2 n_{eq}\lambda} \cdot \frac{2W}{V^2}\left(\frac{dW}{dV}\right)_{TE} \propto \frac{n_f^4 \Delta^{2.5}}{\lambda} \tag{2.18}$$

With an increasing of Δ, the polarization dependence of n_{eq} will increase rapidly, and polarization independence fabrication tolerance can be approximate proportional to $\Delta^{-2.5}$. In Fig. 2-8 shows a polarization independence fabrication tolerance with regard to Δ. In the silicon photonics, with a $\Delta > 40\%$, it is extremely difficult to fabricate polarization independence filter.

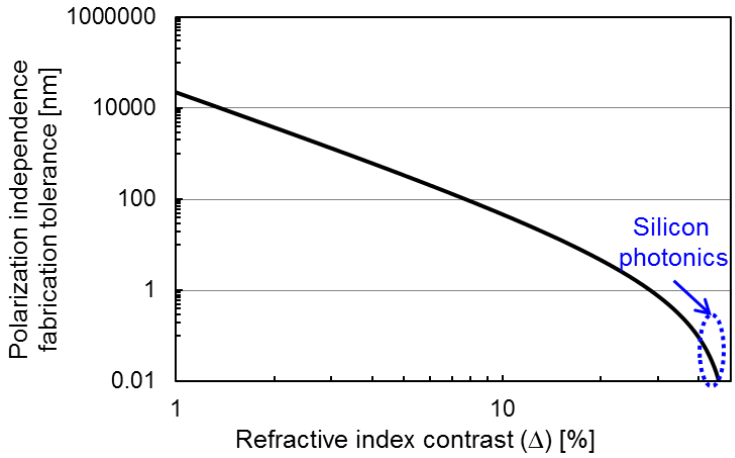


Fig. 2-8 Δ dependence of polarization independence fabrication tolerance.

2.2.2.6 Typical high Δ optical waveguide and task of this study

Recent years, high Δ waveguides made of many kinds of materials have been realized. In semiconductor materials, a typical Si thin wire waveguide [152], InP waveguides [153] and GaAs waveguides [154] have also been reported. As some typical quartz glass materials for PLCs, such as SiON glass [155], Ge doped glass [156] has been reported. Moreover, high Δ waveguide in polymer waveguide [157] have also been studied.

In this work, given a realization of an integrated circuit of a large-volume AOC optical interface over 1 Tbps, in the order of 32 ch x 40 Gbps, but size is less than 1 mm, as shown in Fig. 2-9. What's mean that an optical waveguide with a bending radius (bending loss < 0.1 dB/90^{o}) less than 15 μm must be utilized. Given the analysis method of bending radius of an optical waveguide mentioned in ***2.2.2.2***, and a cladding layer of SiO_2 (n = 1.45), a refractive index of core layer more than 1.8 is necessary, as shown in Fig. 2-10.

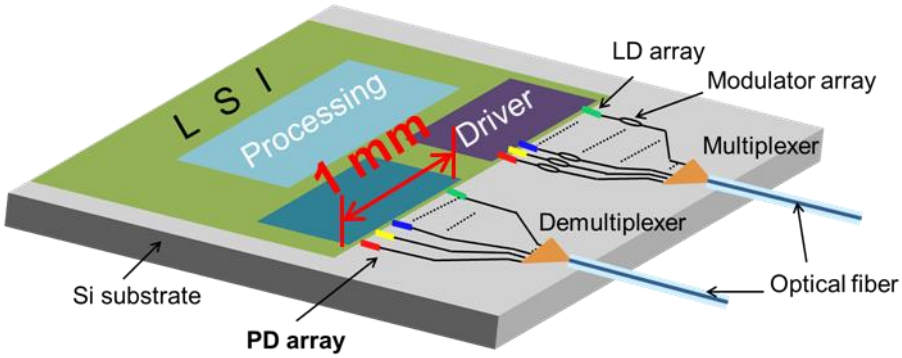


Fig. 2-9 A schematic structure of AOC optical interface.

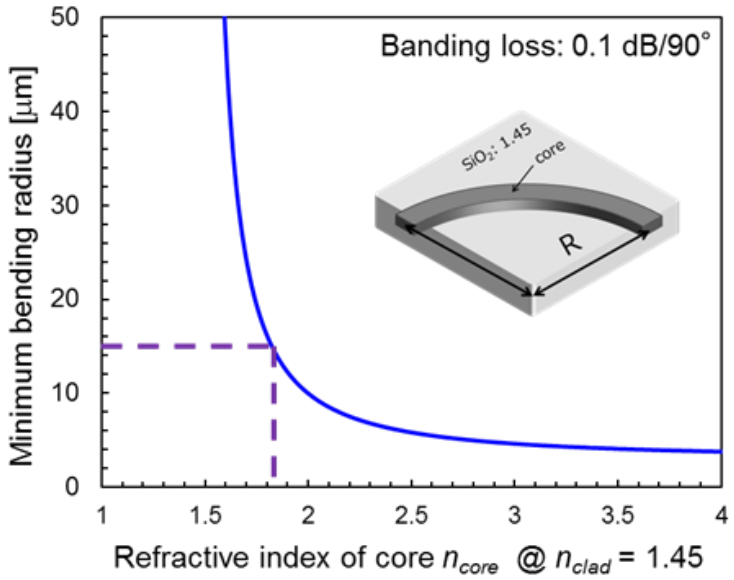


Fig. 2-10 Refractive index of core more than 1.8 for bend radius less than 15 μm (cladding layer of SiO_2: 1.45).

Simultaneously, high dielectric insulator materials have been widely studied for their application in thin film capacitors, which are expected to be used as next generation memory devices [158]. Among these insulators, tantalum pentoxide (Ta_2O_5) is an attractive material for LSIs and optoelectronic devices because of its high resistivity (>10^{12} Ωcm), high breakdown voltage (~1 MV/cm), and high dielectric constant (~25) [159, 160]. Most importantly, Ta_2O_5 has a high refractive index (~2.1) and is considered as a good host material for an optical waveguide amplifier [161]. A Ta_2O_5 thin film strip waveguide, which has been deposited by magnetron sputtering, is demonstrated to be stable when operated in a high-power application (~2 W), with no significant damage to the waveguide, and without an increase in absorption peak intensity over a wide range of wavelengths from 600 to 1700 nm, and the propagation loss is measured at ~1 dB/cm at 1070nm [162]. Therefore, Ta_2O_5 is a promising material candidate, for fabricating high-functional photonic devices, densely embedded in compact photonics integrated circuits for waveguide structures, and is extremely useful for opto-electric integrated circuits (OEICs) in the 0.8 μm wavelength range.

Figure 2-11 shows the structure of multi-mode Ta_2O_5 optical waveguide on a silica substrate, with a waveguide width of 10 μm and thickness of 400 nm.

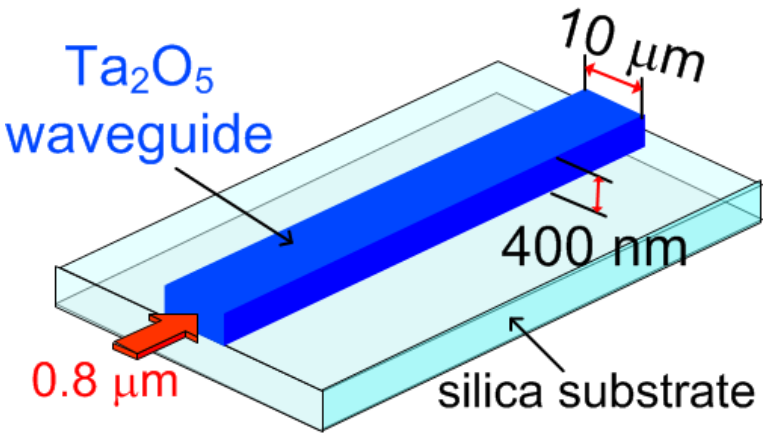


Fig. 2-11 The structure of multi-mode Ta_2O_5 optical waveguide.

The 400 nm thickness of the Ta_2O_5 thin film was determined by the single-mode condition of a slab waveguide with an upper cladding of air (n = 1.0) and a bottom cladding of silica (n = 1.45) in the 0.8 μm wavelength range. Figure 2-12 shows the calculated dispersion curves with TE-mode and TM-mode at λ = 850 nm. The single mode conditions of core thickness are from 78 nm to 425 nm, and 139 nm to 485 nm for TE-mode and TM-mode, respectively.

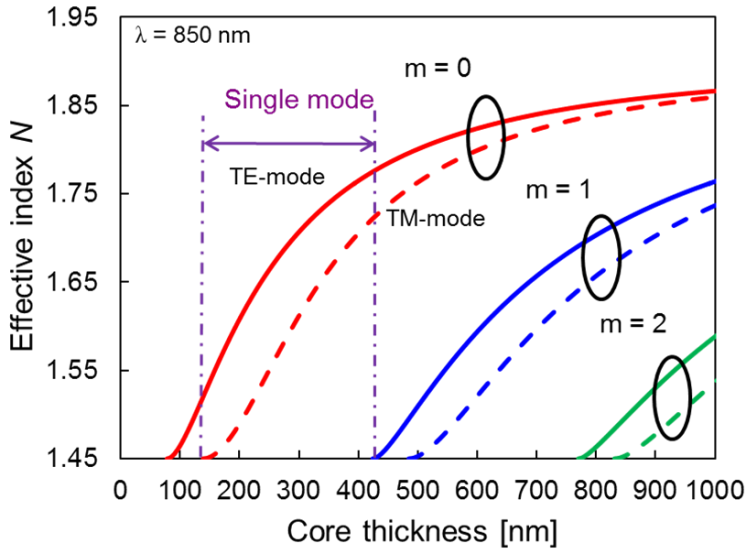


Fig. 2-12 Dispersion curves of Ta_2O_5 optical waveguide at λ =850 nm.

2.3 Fabrication processes of multi-mode Ta2O5 channel waveguide

2.3.1 Overview of fabrication processes

Fabrication process of multi-mode Ta_2O_5 channel waveguide can be summarized as follow, shown in Fig. 2-13. Spin coating method, photolithography and CF_4 reactive ion dry etching were employed, which supplied a cost-effective process.

1. Clean silica substrate with ultrasonic cleaner in acetone 5 min, ethanol 5 min and deionized water 5 min, respectively (Fig. 2-13 (a)).
2. Bake the substrate on hot plate at 120ºC for 5 min to vaporize the water left on the substrate, and cool down for 3 min.
3. Spin coat 1st layer of Ta_2O_5 with 2 steps rotation speed: 1st step 500 rpm 5s, and 2nd step 1500 rpm 60s.
4. Bake the Ta_2O_5 thin film by infrared ramp annealing at 500 ºC 30 min, and cool down for 20 min.
5. Repeat step 3 and 4 for 5 times to get a Ta_2O_5 thickness about 400 nm (Fig. 2-13 (b)).
6. Spin coat a S1830 resist layer with 2 steps rotation speed: 1st step 500 rpm 5s, and 2nd step 5000 rpm 30s.
7. Bake the S1830 resist layer on hot plate at 110 ºC for 10 min, and cool down for 3 min (Fig. 2-13 (c)).
8. UV expose via the photolithography mask 400 W for 40s (Fig. 2-13 (d)).
9. Develop in MF319 for 60s, and deionized water for 30s (Fig. 2-13 (e)).
10. Dry etch the Ta_2O_5 thin film covered a channel waveguide pattern on the S1830 resist layer by CF_4 reactive ion for 120 min, with the condition of RF power of 30 W, gas flow rate of 10 cm^3/min, and pressure of 1.0 Pa (Fig. 2-13 (f)).
11. Remove the S1830 resist layer in acetone 1 min, ethanol 1 min and deionized water 1 min, respectively (Fig. 2-13 (g)).
12. Cut the substrate to obtain desired length of the waveguide.

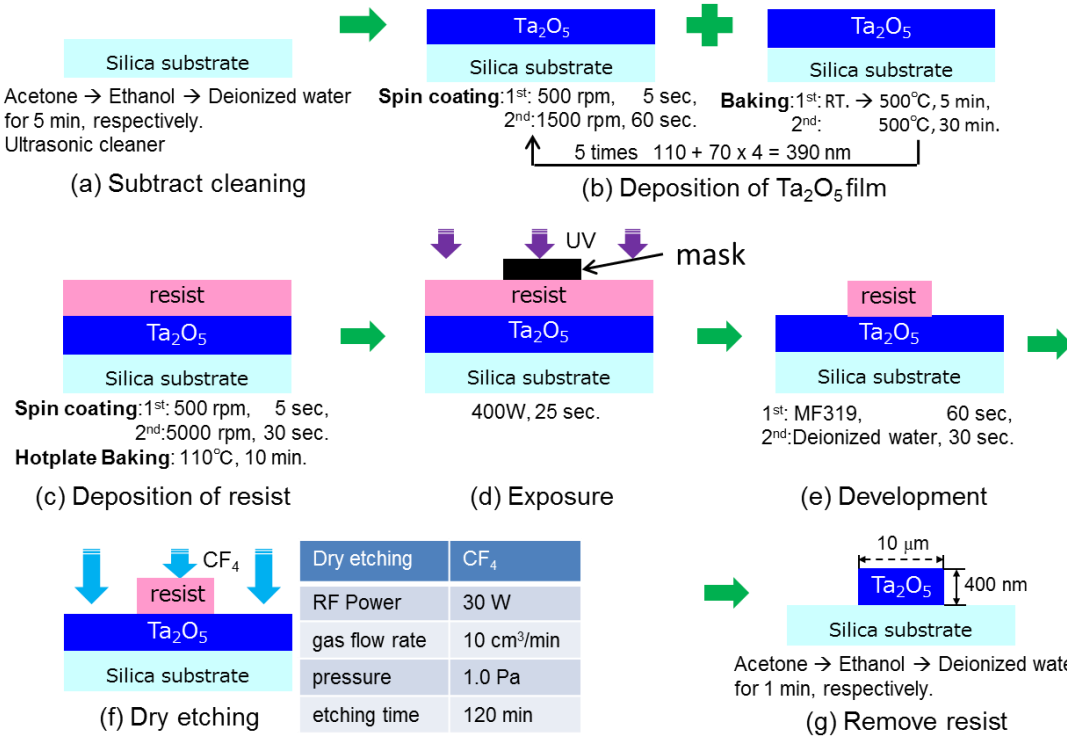


Fig. 2-13 Overview of fabrication processes of multi-mode Ta_2O_5 channel waveguide.

2.3.2 Thin film deposition

A thickness of 400 nm Ta_2O_5 thin film was deposited on a silica substrate by spin coating followed by infrared ramp annealing at 500 ºC for 30 min in atmosphere. Among various deposition methods, such as metal-organic chemical vapor, physical vapor, and chemical solution deposition methods, the chemical solution deposition method has advantages, such as the possibility of working in aqueous solutions with high stoichiometry control. Moreover, it is a low-temperature and cost-effective deposition method owing to its inexpensive precursors and equipment.

In this study, Ta_2O_5 dip-coated precursors with a concentration of 10%, supplied by High Purity Chemicals Ta-10-P, was employed. The silica substrate was pre-cleaned by ultrasonic cleaner in acetone, ethanol, and deionized water for 5 min, respectively.

2.3.2.1 Spin coating

Spin coating process is the process that determines thickness of the Ta_2O_5 core layer. Spin coater used in this study is *SPINCOATER 1H-D2* from *Mikasa Company*. Rotation can be set in two stages, the range of the rotational speed is 0 ~ 9999 rpm, rotation time is 0 ~ 99 sec. On usual, when applying a solution or photoresist, the first stage of spin

coating process is carried out for 5 sec with 500 rpm, to spread the dropped solution over the entire substrate. To get a uniform film, thickness of spin coated film can be depends on spin coating speed and spin coating time of the second stage.

2.3.2.2 Infrared ramp annealing

After the spin coating of Ta_2O_5 solution, baking is carried out to cure the film. Infrared ramp annealing *ULVAC (MILA-3000)* is used in this study. The annealing temperature can be control up to 700 ºC, and it is possible to increase the temperature at a rate up to 2 ºC/s. Moreover, a nitrogen environment can be set up to protect the solution from some chemical reaction under a high temperature.

2.3.2.3 Measurement of film thickness and refractive index

A spectroscopic ellipsometer is used to measure the film thickness and refractive index. The baking temperature and spin coating speed dependences of the film thickness were investigated under the various conditions with baking temperature from 100 ºC to 600 ºC, and the spin coating speed from 1000 rpm to 6000 rpm, while the spin coating time of the second stage and the baking time were constant at 60 sec and 15 min, respectively. The baking temperature dependence of the film thickness is shown in Fig. 2-14, and the spin coating speed dependence of the film thickness is shown in Fig. 2-15. Under the baking time is 15 min, the film thickness become stable around 110 nm when the baking temperature over 400 ºC. It is can be considered that the baking condition with baking temperature over 400 ºC and the baking time over 15 min is stability.

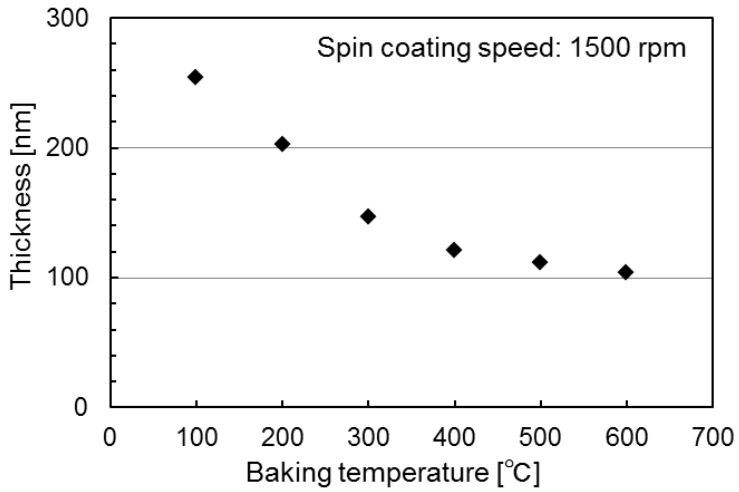


Fig. 2-14 Baking temperature dependence of the film thickness.

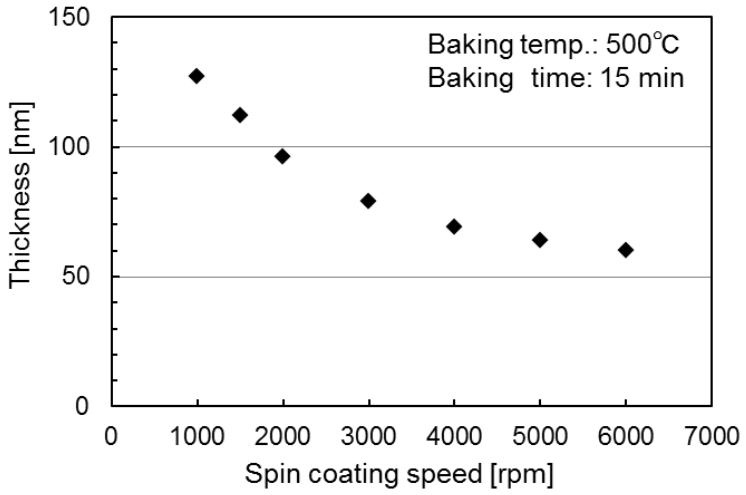


Fig. 2-15 Baking temperature dependence of the film thickness.

Figure 2-16 shows a relationship between spin coating times and film thickness. The first Ta_2O_5 film layer of 110 nm thickness was obtained after the first spin coating of Ta_2O_5 dip-coated precursors onto a silica substrate at a speed of 1500 rpm. Then, a second Ta_2O_5 film layer of about 70 nm thickness was obtained after the second recoating process. It is can be considered that there is a different tackiness between the SiO_2 layer and Ta_2O_5 film, which cause the film thickness differences between the first time deposition when a lower cladding is SiO_2, and a recoating process with the lower subsequent to be Ta_2O_5. The spin coating processes for a 70 nm thickness were repeated up to 3 times until a 400 nm Ta_2O_5 film thickness is obtained.

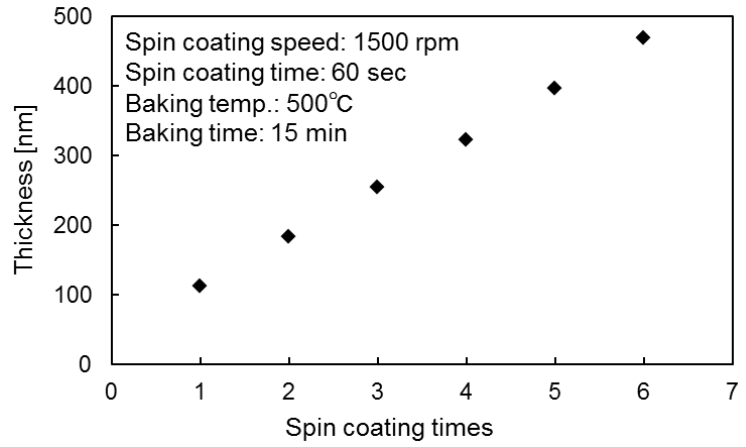
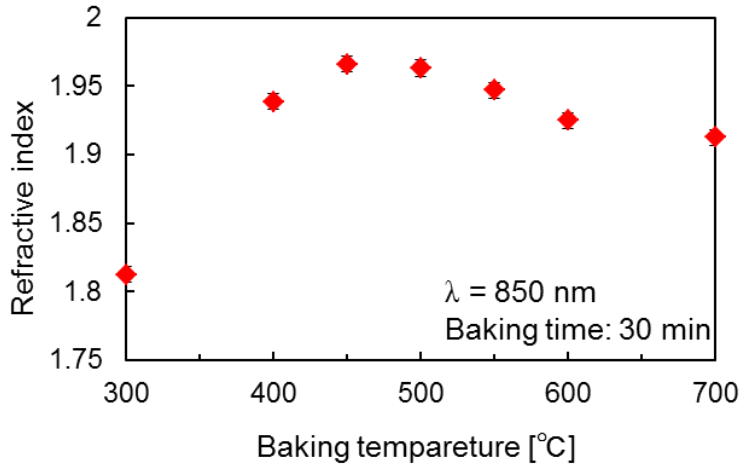


Fig. 2-16 Spin coating times dependence of the film thickness.

The baking temperature and baking time dependences of the refractive index of Ta_2O_5 thin films are shown in Fig. 2-17 (a) and (b), respectively. The error bar shows a standard deviation of the measured values. In the graph, the refractive index of Ta_2O_5 increases markedly with an increase in baking temperature up to 450 ºC. The maximum refractive index of 1.97 was obtained between 450 and 500 ºC. Higher temperatures were not applied as annealing above 600 ºC was reported to form a lossy polycrystalline film [163]. In Fig. 2-17 (b), there are no obvious changes in refractive index at baking times from 5 min to 1 h, but a longer annealing is considered to help reduce losses by filling oxygen deficiencies [162]. On the basis of the above results, annealing using an infrared lamp in atmosphere at 500 ºC for 30 min, with a baking rising rate of 1.6 ºC/s from room temperature, was carried out to bake a wafer. In the heat treatment process, a significant improvement in the transparency of Ta_2O_5 thin films can be observed in atmosphere than in a nitrogen environment, which is similar to a report indicating that post-treatment by annealing in oxygen can reduce propagation losses of Ta_2O_5 waveguides [164].

The Ta_2O_5 thin film thickness and refractive index were measured by spectroscopic ellipsometry in a wavelength range from 400 to 1600 nm, and are shown in Fig. 2-18. A Ta_2O_5 thin film thickness of 396 nm was obtained and a high refractive index of approximating 2.0 in the visible and 0.8 μm wavelength ranges was verified. This value is higher than that of a SiO_2 film, at a refractive index contrast of around 22.3%.



(a)

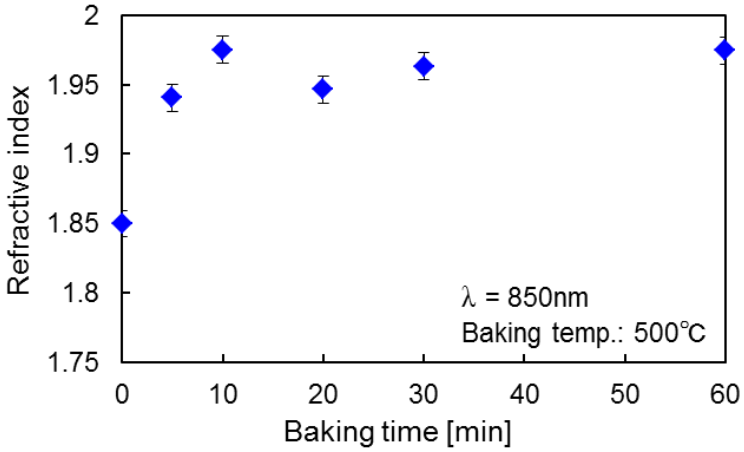


Fig. 2-17 (a) Baking temperature and (b) baking time dependences of the refractive index of Ta_2O_5 thin film.

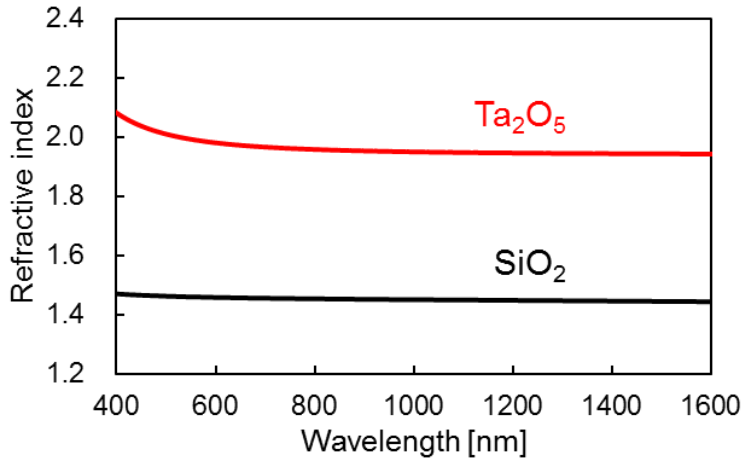


Fig. 2-18 Wavelength dependence of refractive index of Ta_2O_5 film of 396 nm thickness.

2.3.3 Channel waveguide

2.3.3.1 Etching rate

When manufacturing an optical waveguide, an etching fabrication technology is usually employed for producing a ridge-type core. The etching process is a micro-fabrication technology of forming an uneven structure on a substrate by removing portions not covered by the etching mask, as shown in Fig. 2-19. However, in practice, the etching mask may also be etched, in this case until the substrate is etched to the desired depth, it is necessary to remain the mask. The substrate is etched at a constant speed, called etching rate. Etching rate depends on the type of etching gas, varies etching conditions, and the substrate.

$$Selection\ ratio = \frac{Etching\ rate\ of\ the\ substrate}{Etching\ rate\ of\ the\ mask}$$

The selection ratio (SR) is as larger as better when select an etching mask. On the other hand, thinnest thickness of etching mask

$$Mask\ thickness\ \geq \mathrm{SR} \times \text{etching depth}$$

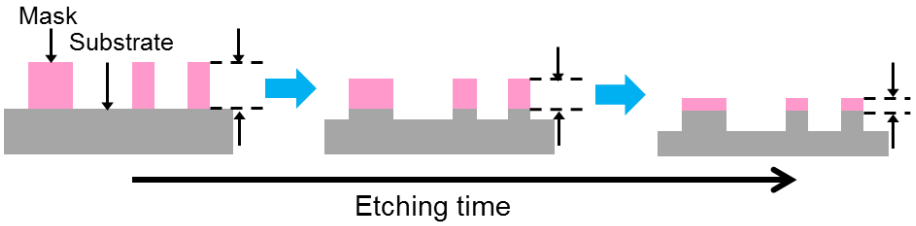


Fig. 2-19 Schematic of a selective etching.

In this study, a selection reactive ion dry etching equipment RIE-10NR (SAMCO) was used. Figure 2-20 shows etching rates of S1830, S1808 and Ta_2O_5 film, with CF_4 flow rate of 10 cm^3/s, pressure of 1.0 Pa, and RF power of 50 W. A selection ratio of about 3 was obtained.

In order to fabricate the strip optical waveguides with a cross section of 400 nm x 10 μm by photolithography with CF_4 reactive ion etching, I used the S1830 photoresist with a 2 μm thickness fabricated by spin coating, which was also used as an etching mask ($0.4 \times 3 = 1.2$ μm thickness was needed) in the dry etching process.

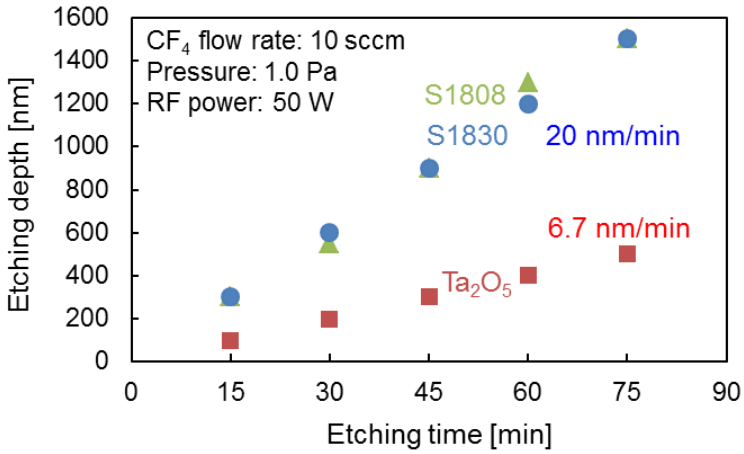


Fig. 2-20 Etching rates of S1830, S1808 and Ta_2O_5 film.

2.3.3.2 UV exposure and MF-319 develop

In this research, the equipment that was used to align the mask and UV exposure is *MASK-ALIGNER M-2L* from *Mikasa Company*. Exposure time can be set to an increment of 0.1 second up to 999 second, and the power of ultraviolet light can be set between 400 ~ 550 W. UV light is exposed to the S1830 photoresist through chrome coated mask which waveguide patterns of 10, 20, 30, 40, 50 μm-widths are written, on exposure condition of 400 Watts 25 seconds. After exposure, the portion exposed was melted in a develop process. When used for the S1808 resist, developing solution MF-319 (TMAH: tetramethylammonium hydroxide) was employed.

UV exposure process is one of the most important processes of Ta_2O_5 waveguide fabrication. Proper UV exposure time and intensity depend on thickness of S1830 photoresist and the width of the Ta_2O_5 waveguide. If exposure of UV light is underexposed, waveguide width may be thicker than the desired value. If over-expose the sample, the width of the waveguide may be slimmer than the desired value, or in the worst case, waveguide pattern may dissolve during developing process. The UV exposure condition will become more important when the pattern is smaller. Many factors (such as exposure intensity, exposure time, contact between mask and the substrate and etc.) must be carefully considered if we want to fabricate pattern with size less than or equal to 1 μm.

2.3.3.3 CF_4 reactive ion dry etching

After patterning, a waveguide height of 400 nm was obtained by CF_4 reactive ion dry etching. The etching rate of 4.1 nm/min in the Ta_2O_5 film was controlled using an RF power of 30 W, a gas flow rate of 10 cm^3/min, and a vacuum pressure of 1.0 Pa, as shown

in Fig. 2-21. Photoresist residues were removed by cleaning similar to the above substrate cleaning.

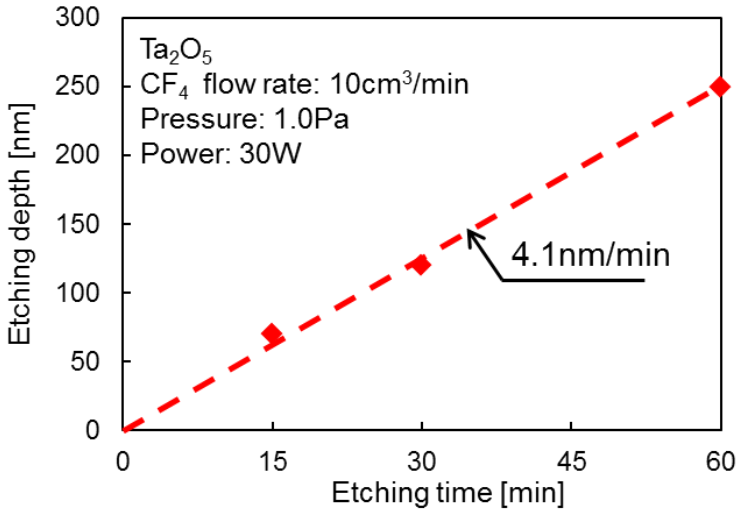


Fig. 2-21 Etching rate of Ta_2O_5 film by CF_4 reactive ions.

2.3.3.4 Sample cutting

Automatic dicing saw machine *DAD322* from *DISCO Company* was used to cut the substrate for observing the cross sectional view of the waveguide, and also, cut the waveguide to the desired length. The samples were placed on a sticky plastic film and cut with the cutting blade. In this experiment, we cut our samples with cutting speed of 0.1 mm/s, blade rotation speed 30000 rpm and cooling water of 0.5 l/m. The cross-sectional view of the Ta_2O_5 waveguide facet is shown in Fig. 2-22. A waveguide width of 10 μm was observed.

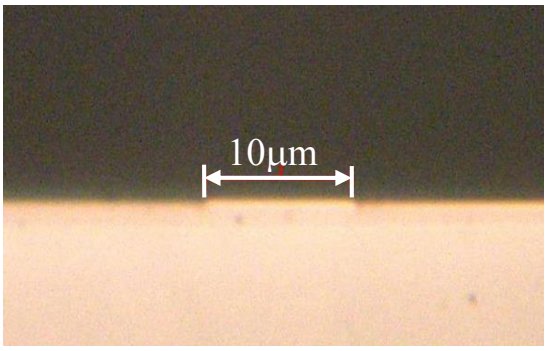


Fig. 2-22 Cross-sectional view of Ta_2O_5 strip waveguide.

2.4 Measurement results and discussions

2.4.1 Measurement system and cut-back method

Optical waveguide losses of the Ta_2O_5 strip optical waveguides were measured by the cutback method at wavelengths of 660, 830, 1310, and 1550 nm. The measurement method is shown in Fig. 2-23. Laser source is connected with a SI-9 lensed optical fiber to coupler light into the waveguide. Then, transmitted light intensity was measured using optical power meter, Hewlett Packard Optical Power Meter 8153A, via a GI-50 optical fiber that was coupled to another end of waveguide. A top view of the propagation of 660 nm light inside the Ta_2O_5 waveguide is confirmed as shown in Fig. 2-24.

Propagation loss was measured using cut-back method. We cut the waveguide into various lengths and measured its propagation loss. In this experiment, 3 waveguides from the same substrate were measured and the waveguides were cut with the length of 2 mm, 3 mm, and 5 mm, respectively.

The optical loss is calculated from following equation:

$$\text{Insertion Loss} = -10\log\left(\frac{P_{out}}{P_{in}}\right)[dB] \tag{2.19}$$

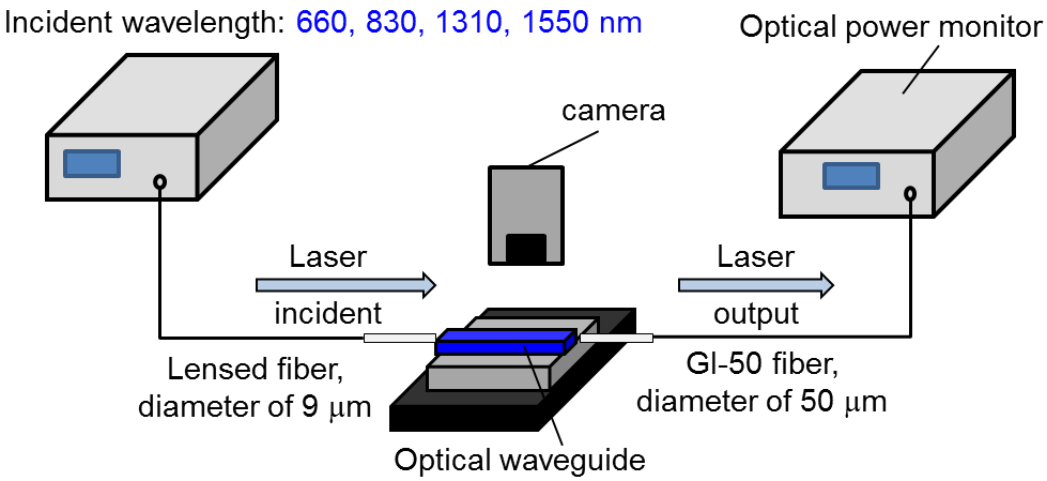
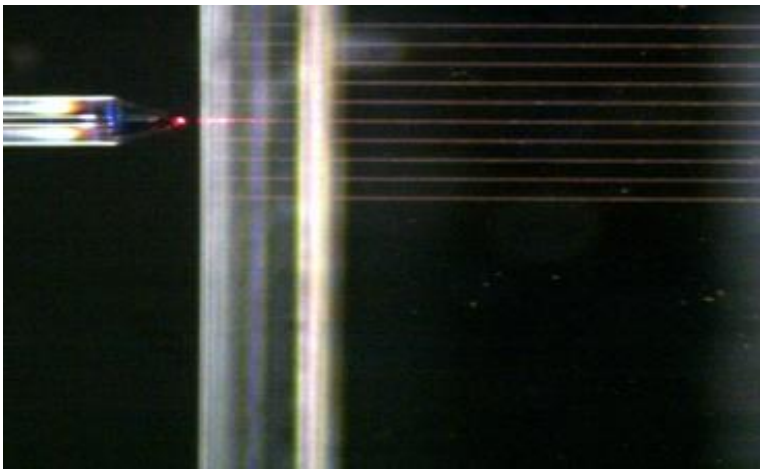
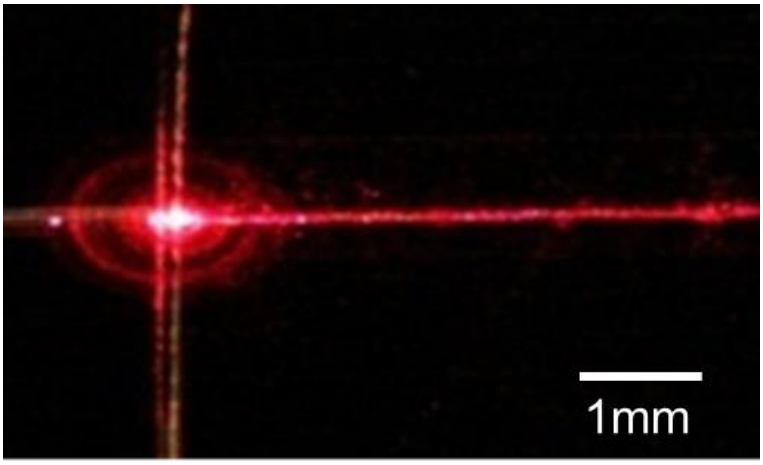


Fig. 2-23 Setup of optical loss measurements.



(a)

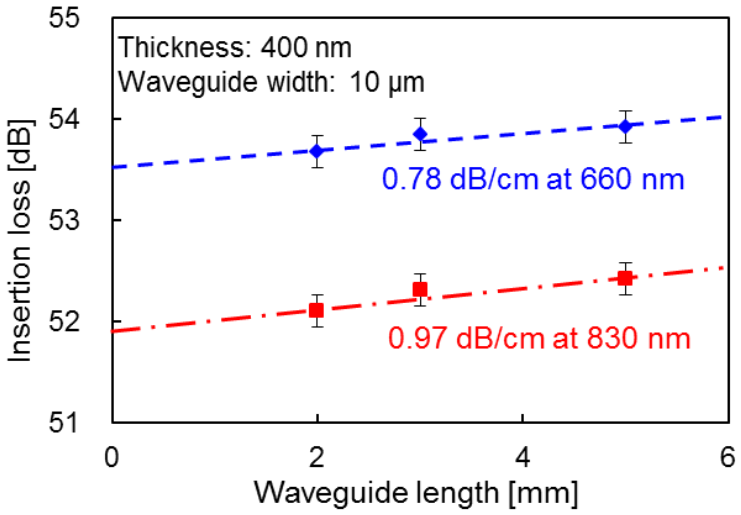


(b)

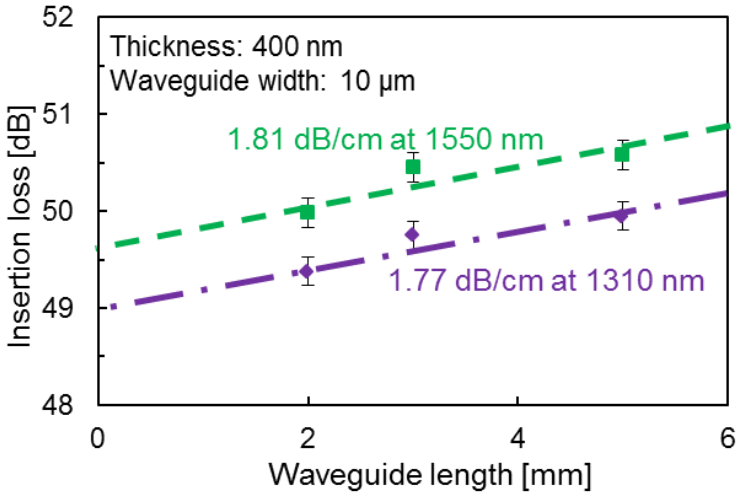
Fig. 2-24 (a) Top view of Ta_2O_5 waveguides. (b) Propagation of 660 nm light.

2.4.2 Experiment results and discussions

The experimental results of insertion losses (sum of propagation and coupling losses) of Ta_2O_5 strip optical waveguides at 660 and 830 nm are shown in Fig. 2-25 (a), and those of 1310 and 1550 nm are shown in Fig. 2-25 (b). The error bar shows a standard deviation of the measured values. A coupling loss can be estimated from the intercept in Fig. 2-28. The coupling losses per facet of 26.8 dB at 660 nm, 26.0 dB at 830 nm, 24.5 dB at 1310 nm, and 24.8 dB at 1550 nm were observed. In addition, the insertion loss of the 3 mm waveguide was observed to be more than that of the 2 or 5 mm waveguide owing to the rough cross section of the 3 mm waveguide compared with the other waveguides. The



(a)



(b)

Fig. 2-25 (a) Insert losses of Ta_2O_5 strip waveguides at 660 and 830 nm. (b) Insert losses of Ta_2O_5 strip waveguides at 1310 and 1550 nm.

propagation losses calculated at various wavelengths are shown in Fig. 2-26. A low propagation loss of less than 1 dB/cm was observed at 830 nm and the lowest propagation loss was 0.78 dB/cm at 660 nm. In comparison with that at short wavelengths, a higher propagation loss, about 1.8 dB/cm, was observed at longer wavelengths. This is because of a lower confinement, in the case of longer wavelengths, causing a higher degree of scattering owing to the surface roughness. In addition to absorption from defects, propagation loss is commonly considered to be caused by the scattered wave, owing to the surface roughness of the waveguide and no uniformity in the core layer. In the case of a Ta_2O_5 waveguide, the scattered wave is not negligible because of a high refractive index contrast between the core and cladding layers. A lower propagation loss is expected owing to an improved reactive ion etching process.

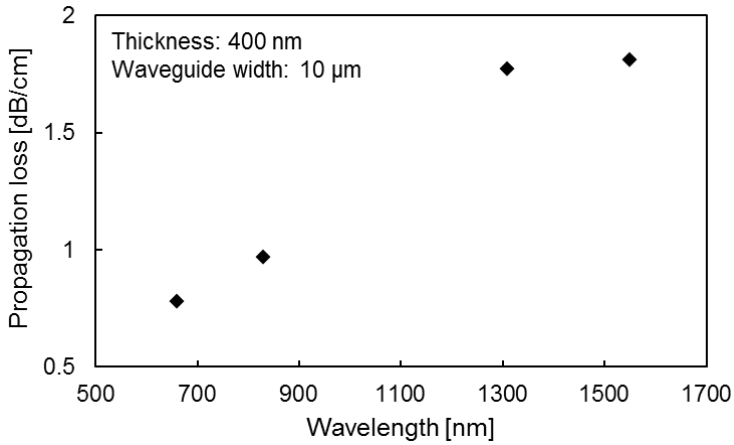


Fig. 2-26 Wavelength dependence of propagation loss of Ta_2O_5 strip waveguides.

2.5 Summary and Future work

In this chapter, a Ta_2O_5 film was formed by a sol-gel method at 500^oC with 30 min annealing on a silica substrate. A refractive index of around 2 was obtained. Ta_2O_5 strip optical waveguides were fabricated by photolithography and CF_4 reactive ion etching, and their propagation loss of less than 1 dB/cm was obtained at 830 and 660 nm. These waveguides can be expected to be employed for OEICs in the 0.8 μm wavelength range.

For the future work, a design and fabrication of single mode Ta_2O_5 optical waveguide have been carried out. Moreover, the advantagements of high Δ optical waveguide is except to be obtained with the implementation of Ta_2O_5-based optical waveguide circuits, such as optical switching, MZI and AWG.

Chapter 3

Waveguide Grating Coupler

3.1 Organization of this chapter

In this chapter, firstly I will introduce a review of coupling techniques between waveguide and photodetector. Especially, a waveguide grating coupler will be discussed in a simple theory analysis.

Then, a directional vertical optical coupler using a Ta_2O_5 optical waveguide grating coupler, which is transparent in the 0.8 μm wavelength range is proposed. The optical waveguide coupler is analyzed by using finite element method (FEM). The coupling efficiency of more than 60% is calculated at the grating period of 530 nm, the duty ratio of 0.5 and the etching depth ratio of more than 0.9 with a thickness of 400 nm, which is the single mode condition of Ta_2O_5 waveguide as mentioned in chapter 2.

3.2 Introduction

3.2.1 Coupling techniques between waveguide and photodetector

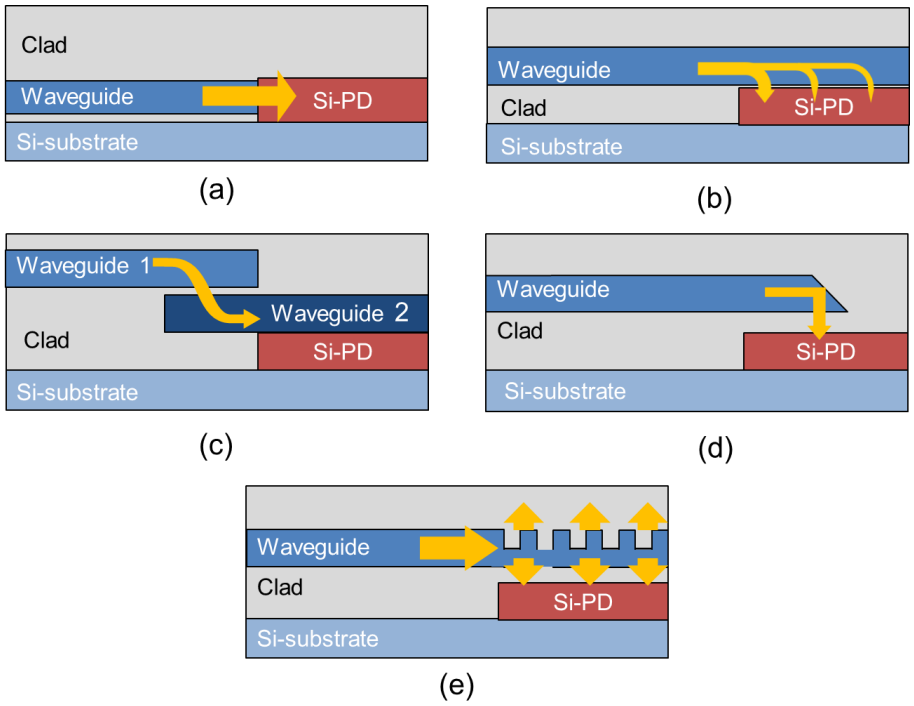


Fig. 3-1 Typical coupling techniques between waveguide and photodetector.

In an optical interconnection, an optical signal is propagated through a waveguide, and it is required to integrate the optical waveguide and a photodetector in a photoelectric conversion unit. Schematic diagram of some typical coupling structures are shown in Fig. 3-1.

Figure 3-1 (a) is a butt-coupling, by adjoining a photodetector to an optical waveguide in the horizontal direction, coupling light from the optical waveguide to the photodetector directly. It is suited to miniaturization of the photodetector because of a high absorption structure. However, the highly accurate positioning technology, and complication of the process are serious challenges. What's more, concentrations of waveguide/photodetector interface light absorption and current generation may reduce a useful life of the element, even occurs some destructions. Si waveguide integrated with a Ge photodiode, or InGaAs photodetector with the butt-coupling was reported [165, 166]. InGaAsP waveguide with InGaAs photodetector is also published in [167].

Figure 3-1 (b) is an evanescent coupling. A photodetector is formed on an optical waveguide layer directly, and the light absorption occurs in the interface by an evanescent wave of the waveguide. A Si waveguide loaded with Ge photodiode, or InGaAs photodetector in this structure was also report [168, 169]. However, these materials are difficult to grow epitaxially on Si substrate because of the lattice mismatch. A wafer bonding technique as one of the approaches to integrate on Si-LSI was reported [170-172]. Owning to using the evanescent wave coupling, it is necessary to control a submicron order (less than 200 nm is expect in the case of Si optical waveguides) bonding thickness between the optical waveguide layer and the photodetector layer. Thus, there is a trade-off between the miniaturization and coupling efficiency.

Figure 3-1 (c) is a two-stage-bound coupling, which can be considered as an improvement of (b), to overcome the lattice mismatch and limited bonding layer thickness. Lightwave is propagated from waveguide 1 to waveguide 2, and light absorption is carried out between waveguide 2 and photodetector with a butt or evanescent coupling. However, from the waveguide coupled-mode theory, the effective refractive indices of waveguide 1 and 2 should be designed to be the same in order to satisfy the phase-matched condition, what is difficult in semiconductor materials owning to larger wavelength dependence than that of silica. A InGaAs photodetector on InP waveguide with an evanescent coupling, two-stage-bound coupling from a Si waveguide [173], and a Ge photodetector with a-Si waveguide butt coupling, two-stage-bound coupling from a Si waveguide [174] are reported.

Figure 3-1 (d) is a mirror reflection. A mirror structure is formed at the end of a waveguide, to provide a 90° bend. As the manufacturing method of waveguide end mirror,

a 90° V-type tip mechanical polishing by a dicing saw [175], or 45°substrate tilted etching [176] was introduced. However, the scattering loss at the waveguide end mirror is a fundamental problem, which cannot be ignored.

Figure 3-1 (e) is a waveguide grating coupling [177-179]. In a planar waveguide and planar photodetector, coupling is made to take place between guided waves propagating in different directions by using a grating structure. For a grating coupler, it is possible for a spacing more than 1 μm between the optical waveguide layer and a photodetector, affording suitable applications between dissimilar materials and multi-layer structure. The loss of light is generated by the grating, the external quantum efficiency decreases in this structure. However, a precise micro-fabrication technology, as 10 nm order, is required to achieve a high efficiency directional diffraction. An InP/InGaAsP PIN photodetector integrated with a SOI waveguide loading grating coupler [180] was reported.

As a common problem, from (a) to (c), there are smaller coupling losses than (d) and (e) in common. Since the light incident direction and the carriers traveling direction are orthogonal, it is possible to improve the responsivity by increasing the photodetector length, without sacrifice the carrier transit time. However, an increase of the photodetector length will also increase the capacity of the photodetector, which cause a limitation of bandwidth and density. In generally, 100 μm or less in detector length is desired. For (d) and (e), there is a trade-off problem between the carrier transit time and the responsivity, because light is incident perpendicular to the photodetector.

3.2.2 Grating components for photonic integrated circuits

Periodic structures or gratings in waveguide are one of the most important elements for PICs, since they can perform various passive functions and provide effective means of guided-wave control [181, 182].

3.2.2.1 Coupling of Optical Waves by Gratings

Figure 3-2 illustrates examples of passive grating components for PICs [183]. They include input/output couplers, waveguide couplers, deflectors, guided-beam splitters, reflectors, mode converters, wavelength filters and dividers, and guided-wave front converters such as waveguide lenses and focusing grating couplers. Periodic modulation of the refractive index can be induced through acousto-optic (AO) and electro-optic (EO) effects. They can be considered a controllable grating, and have many applications to functional devices. Optical coupling by a grating is classified as either guided-mode to guided-mode coupling or guided-mode to radiation-mode coupling, the former

subdivided into collinear coupling and coplanar coupling. Gratings are also classified by structure into index-modulation and relief types, as shown in Fig. 3-3[183].

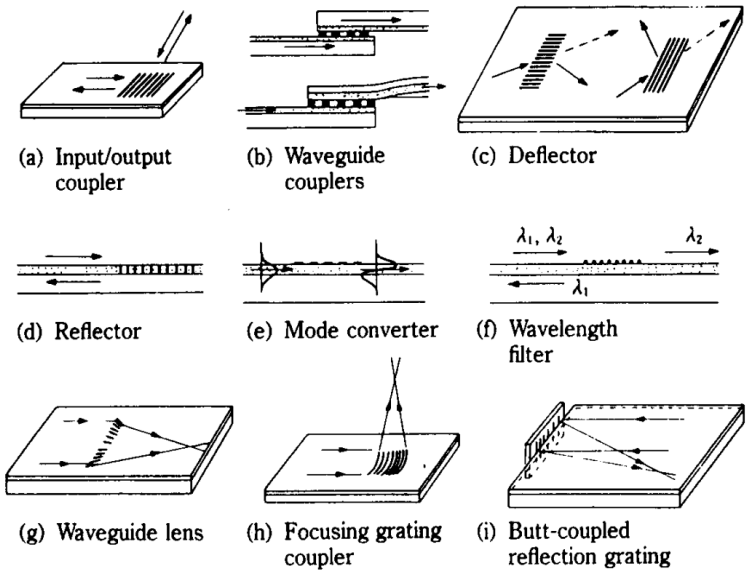


Fig. 3-2 Passive grating components for optical integrated circuits. [183]

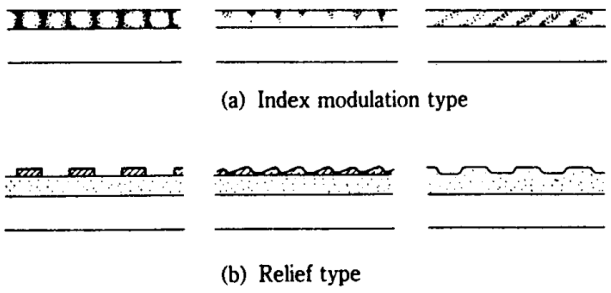


Fig. 3-3 Various cross sections of gratings. [183]

Phase Matching Condition: Various grating structures can be described by the change in distribution of relative dielectric permittivity, $\Delta\epsilon$, caused by attaching a grating to a waveguide. Since the grating is periodic, $\Delta\epsilon$ can be written by Fourier expansion as

$$\Delta\epsilon(x,y,z) = \sum_q \Delta\epsilon_q(x)\exp(-jq\boldsymbol{K}\cdot\boldsymbol{r}) \tag{3.1}$$

using a grating vector $\boldsymbol{K}$ ($|\boldsymbol{K}| = K = 2\pi/\Lambda, \Lambda =$ period). When an optical wave with propagation vector β is incident in the grating region, space harmonics of propagation vectors $\beta + q\boldsymbol{K}$ are produced. The harmonics can propagate as a guided mode, if a coupling condition is satisfied between two waves, a and b, with propagation vectors β_a and β_b.

$$\beta_b = \beta_a + q\boldsymbol{K}, q = \pm 1, \pm 2, \cdots \quad (3.2)$$

In many cases, $\Delta\epsilon$ is nonzero only in the vicinity of the waveguide (y-z) plane, and Eq. (3.2) need not be satisfied for the x component. Each part of Eq. (3.2) is called a *phase matching condition*, while the three-dimensional relation is called the *Bragg condition*. The relation can be depicted in a wave vector diagram, which is used to determine the waves involved in the coupling.

3.2.2.2 Principle of Guide-Mode to Radiation-Mode Coupling

Output Coupling: Figure 3-4 [183] illustrates the coupling between a guided mode and radiation modes. Coupling takes place between waves satisfying phase matching for z components. When a guided wave of propagation constant β_0 is incident, the q_{th} harmonics radiate into air and/or substrate at angles determined by

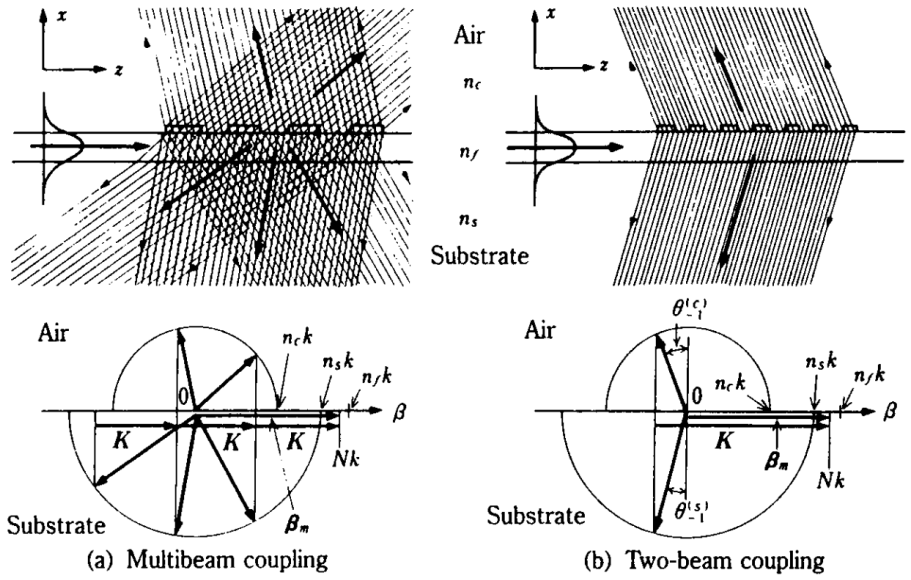


Fig. 3-4 Guided-mode and radiation-mode coupling in a grating coupler. [183]

$$n_c k sin\theta_q^{(c)} = n_s k sin\theta_q^{(s)} = \beta_q = Nk + qK \quad (3.3)$$

The number of radiation beams is determined by the number of real values of $\theta_q^{(s)}$ and $\theta_q^{(c)}$ satisfying Eq. (3.3). An order results in radiation into either the substrate alone or both air and substrate. Figure 3-4 (a) shows multibeam coupling where more than three beams are yielded and Fig. 3-4 (b) shows two-beam coupling where only a single beam for the fundamental order ($q = -1$) is yielded in both air and substrate. Another

possibility is one-beam coupling where a beam radiates only into the substrate. The amplitude of the guided and radiation wave decays as $g(z) = exp(-\alpha_r L)$ due to the power leakage by radiation. Since the guided-wave attenuation corresponds to the power transferred to radiation modes, the output coupling efficiency for a grating of length L can be written as

$$\eta_{\text{out}} = P_q^i\{1 - \exp(-2\alpha_r L)\} \tag{3.4}$$

for the qth-order (i) radiation, where i (equal to c or s) distinguishes air and substrate. Here α_r denotes the radiation decay factor and P_q^i is the fractional power to q-I radiation.

Input Coupling: A guided wave can be excited through reverse input coupling of an external beam incident on a grating. When the incident angle coincides with one of the angles satisfying Eq. (3.3), one of the produced space harmonics synchronizes with a guided mode and the guided mode is excited. Figure 3-5 [183] correlates output and input couplings. A reciprocity theorem analysis shows that the input coupling efficiency can be written as

$$\eta_{\text{in}} = P_q^i \cdot I(g,h) \quad I(g,h) = \frac{[\int ghdz]^2}{\int g^2 dz \int h^2 dz} \tag{3.5}$$

where $h(z)$ is the input beam profile. The overlap integral $I(g,h)$ takes the maximum value 1 when the beam profiles are similar $[h(z) \approx g(z)]$. Practically, high efficiency can be achieved by (1) making a grating of $\alpha_r L \gg 1$, (2) making $P_q^i \approx 1$ for one beam q, i, and (3) feeding an input beam satisfying $h(z) \approx g(z)$. For an input beam with *Gaussian* profile, the maximum value of $I(g,h)$ is 0.801.

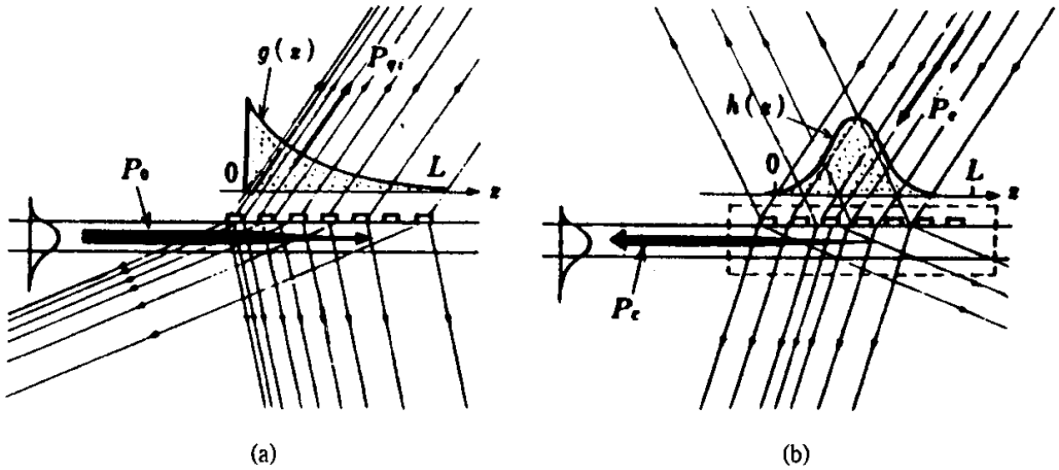


Fig. 3-5 Input and output coupling by a grating: (a) Output coupling, (b) Input coupling. [183]

Radiation Decay Factor: The radiation decay factor α_r can be calculated by various methods, e.g., a coupled-mode analysis, a rigorous numerical analysis to calculate the complex propagation constant of normal modes by space harmonics expansion based on *Floquet*'s theorem, and approximate perturbation analyses based on a *Green*'s function approach or a transmission-line approach. Figure 3-6 [183] illustrates typical dependence of the decay factor α_r of couplers of the relief type on the grating groove depth *h*. For small *h*, α_r increases monotonously with *h* and is approximately proportional to h^2. For larger *h*, the coupling saturates because of the limited penetration of the guided-mode evanescent tail into the grating layer. In the saturation region, interference of the reflection at upper and lower interfaces of the grating gives rise to a weak periodic fluctuation.

High-Efficiency Grating Couplers: One-beam coupling is desirable to achieve high efficiency. Such coupling can be realized by using backward coupling by a grating of short period. Two-beam couplers, as shown in Fig. 3-4 (b), are more widely used, but they have the drawback that the power is halved for air and substrate. The drawback can be eliminated by inserting a reflection layer on the substrate side. Methods for confining the power into single *q* and *i* include use of the Bragg effect in a thick index-modulation grating, and use of the blazing effect in a relief grating having an asymmetrical triangular cross section.

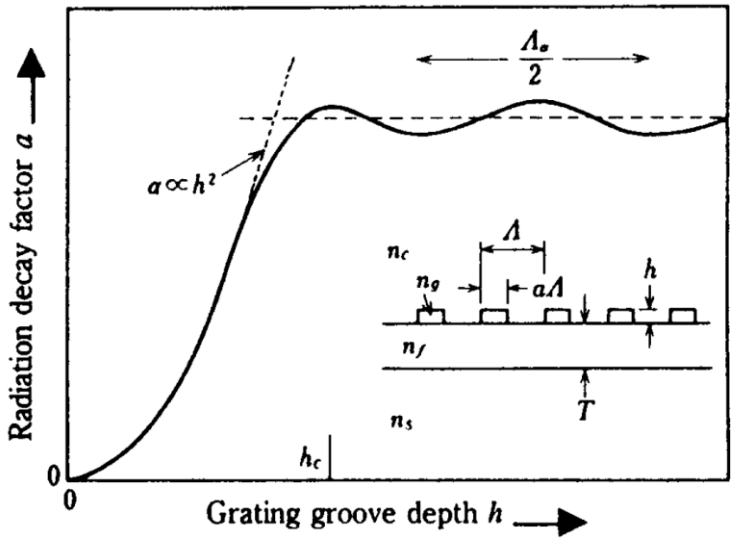


Fig. 3-6 Dependence of radiation decay factor on the grating groove depth for grating coupler of the relief type. [183]

3.2.3 Applications of input-output waveguide grating coupler

In the field of OEICs, a polarization insensitive grating coupler had been measured less than 0.89 dB of difference between TE and TM mode lightwave [184]. In past studies, grating couplers has been used to realize the coupling between fiber and optical waveguides [185-189]. An out-of-plane grating coupler for efficient butt-coupling from single mode fiber to compact planar waveguides, by using a short second-order grating has been optimized by using mode expansion-based simulation and trial fabricated. As a result, up to 74% coupling efficiency was possible by a 2-D simulation and had measured 19% coupling efficiency on a test structure [190]. What's more, A coupling efficiency >30% with a 1 dB bandwidth of 40 nm had experimentally demonstrated and the coupling efficiency can be improved theoretically to > 90% using an optimized grating design and layer stack [191]. For more, a high-efficiency grating couplers for coupling between a single-mode fiber and nanophotonic waveguides with an adiabatic taper, had been simulated and fabricated, and the measured coupling efficiency to fiber was 69% for SOI grating couplers [192].

On the other hand, in order to realize three-dimensional (3D) optical circuits along with multi-stacked layers, a high-index-contrast vertical grating coupler based on hydrogenated amorphous silicon (a-Si:H) had also been demonstrated. The distance between the multilayer waveguides was fixed to 1 μm for an optical isolation, and the maximum coupling efficiency was estimated to be 22% from the measurements in the C-band [193].

3.3 Design description

3.3.1 Vertical direction waveguide grating coupler

For a description of the vertical coupler, the diffraction grating acts as a source to diffract the transmitting light wave. If the origin of the diffraction is periodic, the diffracted waves add together in a specific direction and strong scattering or diffraction occurs. Figure 3-7 shows the diffraction of the light which is incident from the left bottom at an angle θ_i , upon a waveguide-type diffraction grating. The diffraction angle is expressed as θ_m. The phase of the wave front is constant between A and A' before scattering, and B and B' after scattering. When the distances $\overline{A'B} - \overline{AB'}$ is consistent with an integer multiple (N) of the wavelength in the medium, from the Bragg condition, we can get an equation as:

$$cos\theta_m = \cos\theta_i \mp \frac{2N}{m}\left(\frac{n_{eq}}{n_2}\right) \tag{3.6}$$

where n_{eq} is the equivalent refractive index of waveguide grating, n_2 is the refractive index of cladding, *m* is called lattice order [194]. From the equation, θ_m is possible to be 90°, what mean a vertical direction waveguide grating coupler.

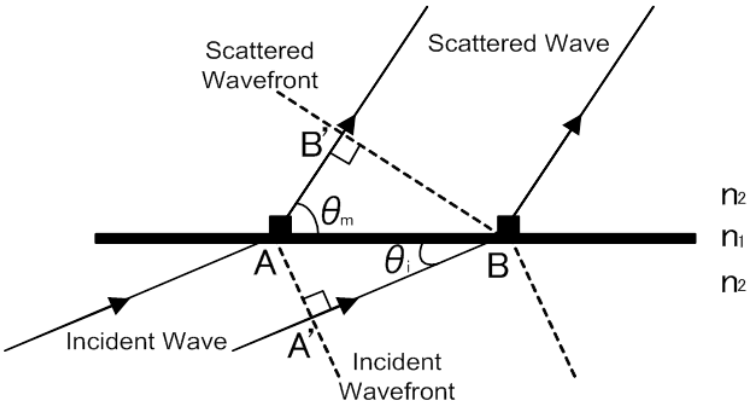


Fig. 3-7 Schematic of Scattered waves from a waveguide grating.

3.3.2 Parameters and numerical modeling of waveguide grating coupler

The design structure of the diffraction grating coupler is shown in Fig.3-8. Here we simplify the Si-PD layer into a power monitor. On the detector, a SiO_2 layer, with a thickness of 2 μm is placed as the under cladding layer. A Ta_2O_5 waveguide with a diffraction grating structure is fabricated on the SiO_2 layer. The thickness of core layer is fixed on 400 nm, which is decided by the single mode analysis as mentioned in chapter 2. The upper cladding layer is air with a thickness of 2 μm.

For the simulation, we can count out the energy intensity of scattered wave by the diffraction grating coupler from a power monitor P_{det}, and the coupling efficiency is calculated by dividing the power of detector into the incident P_{in}, as:

$$\eta = \frac{P_{det}}{P_{in}} \tag{3.7}$$

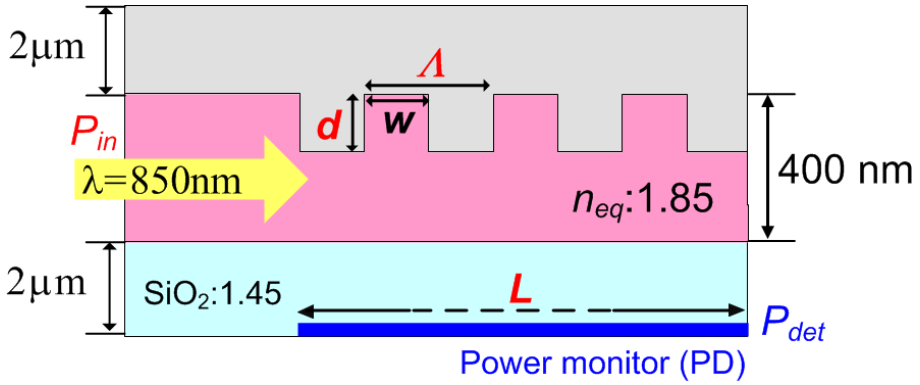


Fig. 3-8 Analytical model of Ta_2O_5 waveguide grating coupler

The incident wavelength and the refractive index of cladding layer are 850nm and 1.45 for SiO_2. The equivalent refractive index of the core layer is calculated to be 1.85 by equivalent refractive index method, what is useful to approximate a channel waveguide into two-dimensional view. The initial parameters used in the simulation are shown in table 3-1, and the grating period (Λ), duty cycle (w/Λ), and etching depth (d) dependences of the coupling efficiency, diffraction angular were analyzed.

Table 3-1 Parameters used in the simulation of grating coupling.

Grating period (nm)	Duty cycle	Etching depth ratio	Grating length (μm)
Λ	w/Λ	d	L
450 ~ 650	fix to 0.5	0.8 ~ 1.0	5 ~ 50

3.3.3 Evaluation method

The numerical simulation of optical propagation in diffraction grating structure is analyzed by the two-dimensional finite element method (FEM), using *RF module 4.2 of COMSOL Multiphysics*.

COMSOL Multiphysics is a finite element analysis, solver and Simulation software/FEA Software package for various physics and engineering applications, especially coupled phenomena, or multiphysics. *COMSOL Multiphysics* also offers an extensive interface to *MATLAB* and its toolboxes for a large variety of programming, preprocessing and post-processing possibilities. The packages are cross-platform (*Windows, Mac*, and *Linux*). Many modules are integrated with software including RF modules which was used in this research.

3.4 Simulation results and discussions

3.4.1 Structure and grating period dependency

Figure 3-9 shows the structure dependence of coupling efficiency with variable grating periods. Here, the etching depth ratio and duty cycle is fixed to be 1.0 (completed etching) and 0.5. The differences of structural design are shown in Fig. 3-9 (a) and (b), compared to a symmetric structure in Fig. 3-9 (a) with a cladding layer of SiO_2, an asymmetric structure in Fig. 3-9 (b) with only bottom cladding layer of SiO_2 was designed to expect to achieve a higher bottom directional coupling efficiency. From Fig. 3-9 (c), the coupling efficiency significantly reduced at the grating period of 540 nm and 590 nm, respectively, which are marked for Λ_B, mean Bragg periods, because of a strong Bragg reflection. It happens when the period of diffraction grating is consistent with the Bragg period. On the other hand, if there is a little deviation from the Bragg period, the coupling efficiency could take the maximum value, and the vertical scattered wave can

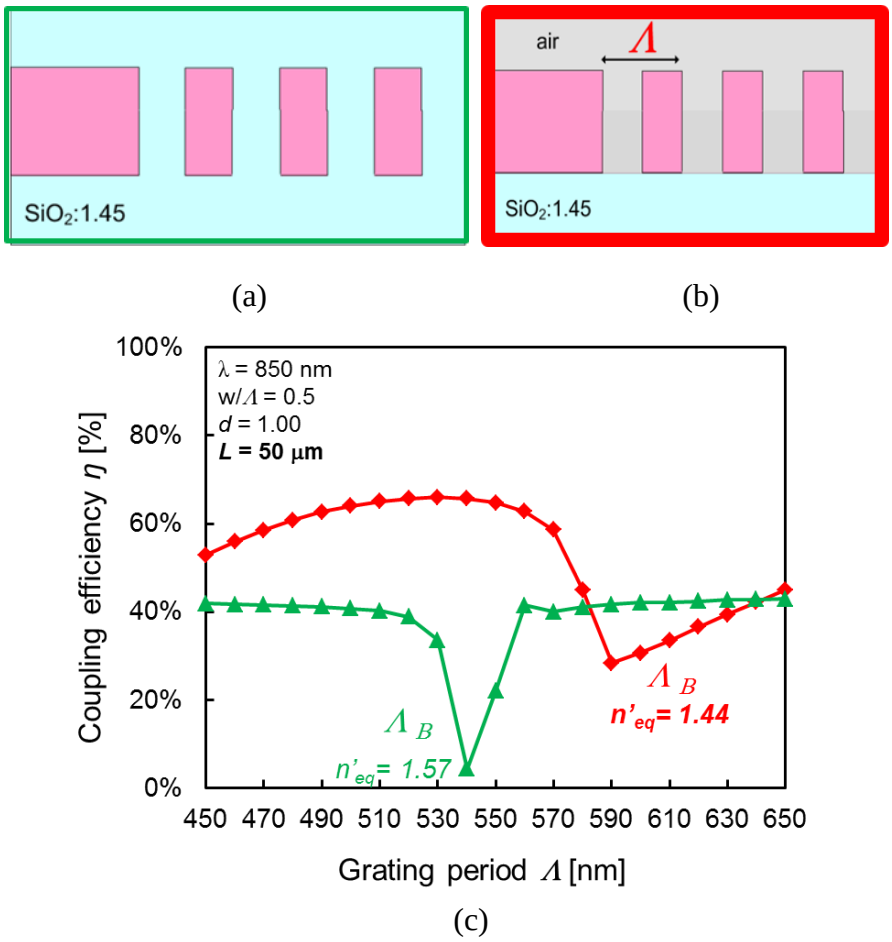
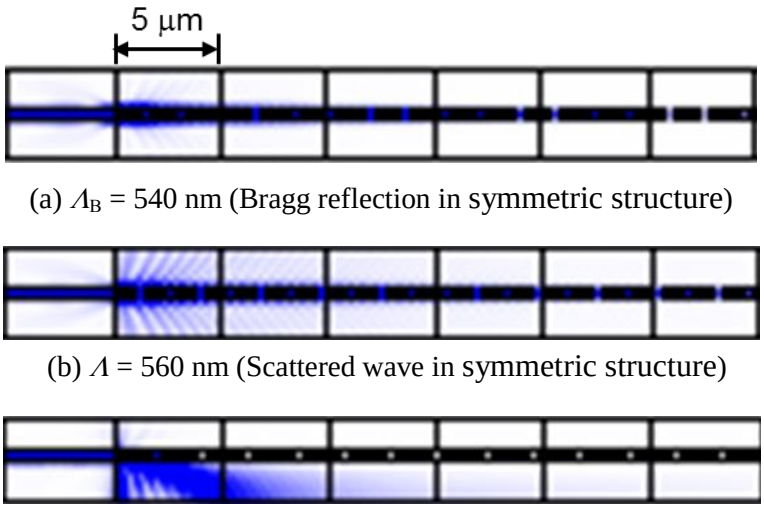


Fig. 3-9 Structure and grating period dependences of coupling efficiency.



(a) Λ_B = 540 nm (Bragg reflection in symmetric structure)

(b) Λ = 560 nm (Scattered wave in symmetric structure)

(c) Λ = 530 nm (Scattered wave in asymmetric structure)

Fig. 3-10 Reflection and scattered wave power in symmetric and asymmetric structure.

also be confirmed by the result of simulation as showed in Fig. 3-10. What's more, it can be estimated from the Bragg periods, that the equivalent refractive index of the waveguide grating coupler is 1.57 in symmetric structure and 1.44 in asymmetric structure, respectively. What's more interesting, in the case of the equivalent refractive index of the waveguide grating coupler is 1.44, even smaller than the refractive index of bottom cladding layer SiO_2 (n = 1.45), a stronger bottom directional coupling effect was demonstrated, as the same as shown in Fig. 3-11.

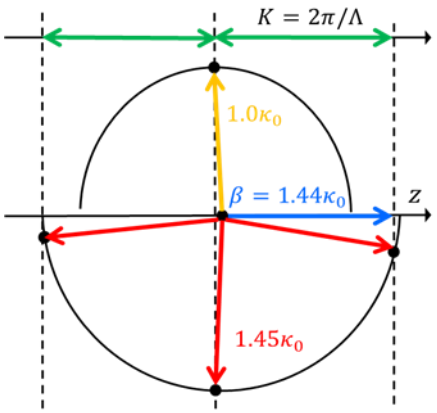


Fig. 3-11 Increase of bottom coupling efficiency by utilizing asymmetric structure.

3.4.2 Grating length dependency

Figure 3-12 (a) shows the grating length dependency of the bottom directional coupling efficiency, when the etching depth ratio and duty cycle is fixed to be 1.0 and 0.5. The grating period is employed 530 nm both in the symmetric and asymmetric structures. Given the grating length from 0 to 50 μm, the bottom directional coupling efficiency is increasing slowly in the symmetric structure, and gets a maximum coupling efficiency about 35%. Compared to the symmetric structure, an asymmetric structure exhibits a saturating grating length of 15 μm, with a maximum coupling efficiency of 62.8%, which is potential to realize compact integrated optical circuits. Figure 3-12 (b) and (c) shows the electric field distribution in the both structures.

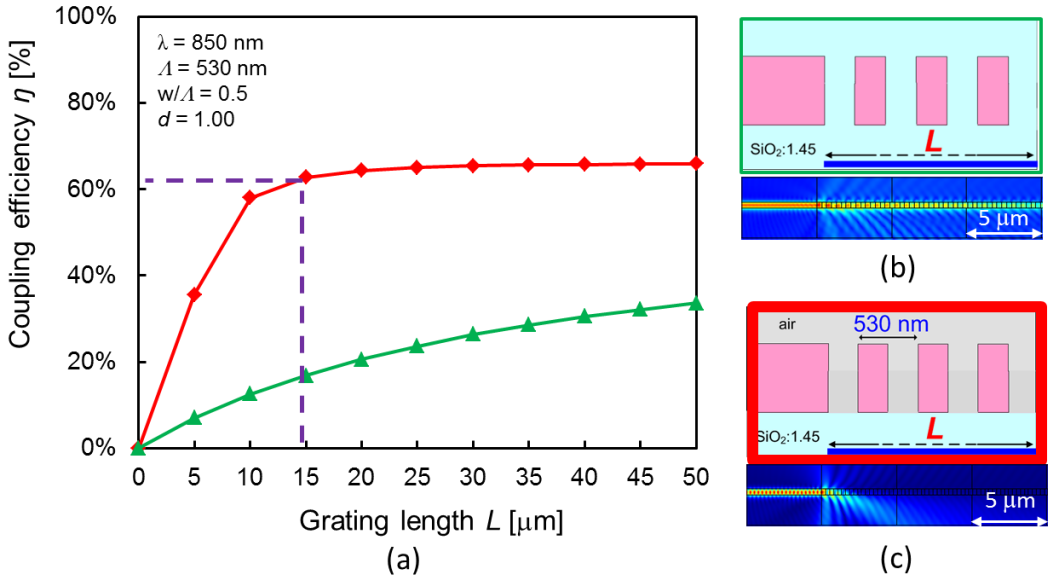


Fig. 3-12 Grating length dependence of bottom directional coupling efficiency.

3.4.3 Wavelength dependency

Figure 3-13 shows the wavelength dependence of the bottom directional coupling efficiency, when the etching depth ratio and duty cycle is fixed to be 1.0 and 0.5. Here, the grating period and grating length is fixed to 530 nm and 15 μm, respectively, in the asymmetric structure. While the wavelength is from 800 nm to 900 nm, the maximum coupling efficiency of 66% at 823 nm, and the minimum coupling efficiency of 57% at 900nm. In the case of grating length of 15 μm, the coupling efficiency exhibit only 0.65 dB loss for 100 nm.

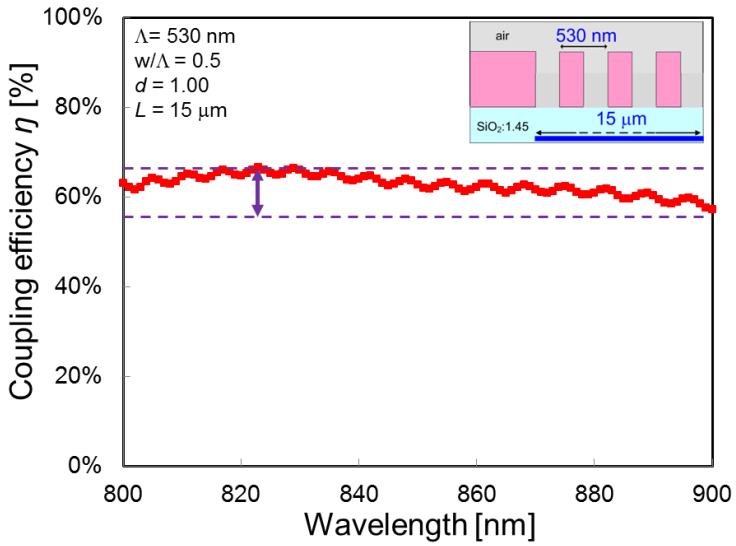


Fig. 3-13 Wavelength dependence of bottom directional coupling efficiency.

3.4.3 Etching depth ratio dependency

Given a fabrication tolerance, the etching depth ratios from 0.8 to 1.0 of bottom directional coupling efficiency were investigated, when the grating period and duty cycle is fixed to 530 nm and 0.5, respectively, in the asymmetric structure, as shown in Fig. 3-14 (a). Figure 3-14 (b) shows the grating length dependency with various etching depth ratios. While the etching depth is getting thinner, the maximum coupling is reduced, owing to an attenuation of asymmetric structure; and the Bragg period shift to be shorter wavelength, because an increase of the equivalent refractive index of the whole grating coupler.

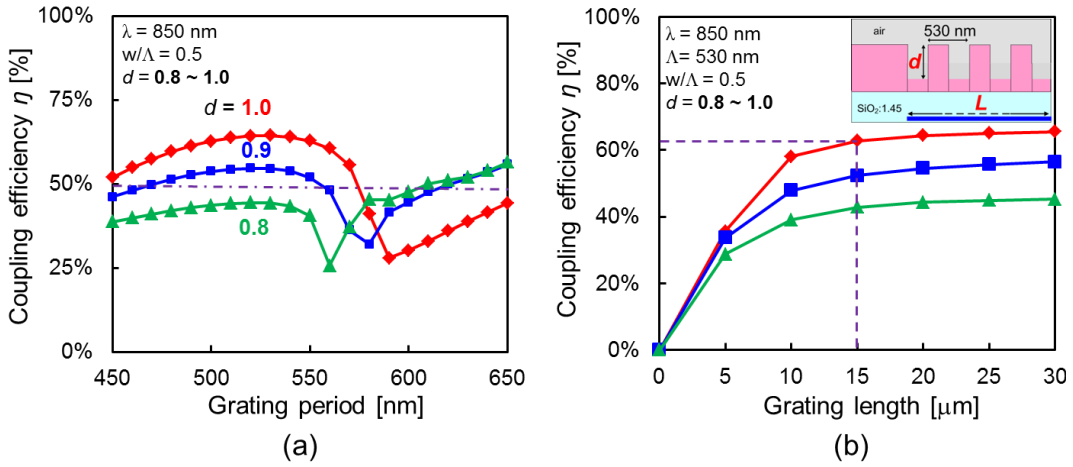


Fig. 3-14 Etching depth ratio of bottom directional coupling efficiency.

3.5 Summary and Future works

In order to solve the problem of optical coupling between waveguide and planar photodetector, I proposed and simulated a high-efficient vertical directional grating coupler between the Si-PD and Ta_2O_5 waveguide. In the study of Ta_2O_5 waveguide grating coupler, we can see that the directional diffraction wave has a high dependence on the asymmetric structure, and we can get a bottom directional coupling efficiency over 60% in a grating length less than 15 μm and wavelength more than 80 nm. The short coupler length (less than 15 μm), but high efficiency is considered due to the combination of the high refractive index of Ta_2O_5 and the asymmetric structure.

For the future work, a design of non-equal intervals or lensed effect waveguide grating coupler has been carried out. By design a non-equal intervals grating, reduces of the refractive wave and less wavelength dependence can be expect. By design different grating periods, the direction of diffraction wave can be controlled to achieve a lensed effect in the same waveguide coupling, which is expect to reduce a coupling length significantly.

Chapter 4

Lateral Silicon Photodetector

on Silicon-on-insulator Substrate

4.1 Organization of this chapter

In this chapter, firstly I will introduce a review of the improvement and performance comparison of photodetector on silicon, especially, Si photodetectors.

Then, a Si photodetector with a structure combining the advantages both of SOI and lateral p-i-n PD, fabricated in a CMOS compatible process was proposed. In addition, we discussed structure dependences on the frequency and an optimum design for the maximum bandwidth.

4.2 Introduction

4.2.1 Semiconductor photodetector on silicon

Over the last two decades InP with its lattice-matched compounds has proved itself to be the most appropriate material system for the fabrication of high-performance photodiodes in the C and L bands. Owing to its good material quality, high absorption efficiency, and high carrier drift velocities, the InGaAs/InP photodiode has become a standard solution for today's high-speed applications.

However, concomitant with the rapid advances in Si photonics there has been considerable research toward the integration of high-speed photodiodes on silicon-on-insulator (SOI)/Si substrates. Although Si is transparent at wavelengths >1.1 μm numerous approaches have been reported to enable efficient light detection at 1.55 μm wavelength, including ion-implanted all-silicon [195], InGaAs/GaAs growth on Si [l96, l97], polycrystalline Ge films [198, 199], Si-Ge hetero-epitaxy [200-202], and III-V on Si bonding [203].

High-speed Ge photodiodes: Germanium is a viable absorber material for high-performance photodiodes as it provides sufficient absorption up to ~ 1550 nm wavelengths. Depending on growth conditions and strain, absorption coefficients between 1000 cm^{-1} and 4000 cm^{-1} at 1.55 μm wavelength have been reported [204, 205]. Ge can be grown on Si; however, the main difficulty is the ~ 4% lattice mismatch between Ge and Si which can lead to high defect densities in the Ge [212]. These defects may

cause high dark current, which would compromise the sensitivity of the photodiode. The amount of dark current that can be tolerated depends on the bit rate [206] and application; however, it has been suggested that < 1 μA is typically sufficient for high-speed receivers [207]. Growth techniques including the deposition of graded SiGe buffer layers, high/low temperature growth [201], area-selective growth [208, 209], and cyclic annealing have been shown to effectively improve material quality [210]. Several low dark current Ge on Si photodiode has been presented [211]; however, the problem with high dark current persists to some extent.

Recently, surface-normal photodiodes that reached a bandwidth of 36 GHz, responsivity of 0.47 A/W, and low dark current < 100 nA have been demonstrated [211]. A 10 μm-diameter n-i-p photodiode, grown by a two-step technique using MBE, achieved a high bandwidth of 49 GHz was reported [212]. Waveguide photodiodes can achieve higher bandwidth-efficiency products and to date several high-performance Ge waveguide photodiode have been demonstrated [213, 214]. By their nature they have become important devices in SOI/Si photonic integrated circuits. Recently, research has focused on CMOS-compatible processing techniques for Ge waveguide photodiodes [207, 215]. The goal is to enable large-scale photonic-electronic integration using the available CMOS infrastructure. However, the thermal budget of the Ge epitaxy and postgrowth annealing is still one critical issue for CMOS integration [216]. Another requirement arises from the fact that both detector and the electronic circuit should operate on a single power supply < 1.5 V [217]. Ideally, zero-bias operation is desired, not only to minimize dark current but also to reduce power consumption.

The latest, a butt-coupled lateral p-i-n photodiode with > 110 GHz bandwidth was reported [218]. A 10 x 10 μm^2 silicon recess was etched at the end of the 500 nm wide Si waveguide and Ge was selectively grown by RP-CVD. Boron and phosphorus were implanted to form a horizontal p-i-n junction with a nominal intrinsic Ge width of 500 nm. The responsivity was 0.8 A/W at 1.55 μm and open eye diagrams at 40 Gb/s were obtained under zero-bias operation.

Heterogeneously integrated III-V photodiodes on Si: Wafer bonding of III-V material on Si has been shown to be a viable technique to integrate dissimilar materials without compromising their properties [219-223]. While this approach is particularly interesting for silicon transmitters [224], it may also lead to low dark current photodiodes with high efficiencies beyond 1.55 μm. Park et al. reported an evanescently-coupled waveguide photodetector utilizing AlGaInAs quantum wells bonded to a SOI waveguide [225]. The photodetector had fiber-coupled responsivity of 0.31 A/W and 0.23 A/W at 1.55 μm and 1.65 μm wavelengths, respectively, an internal quantum efficiency of 90% at 1.55 μm,

and a dark current <100 nA at 2V. Using the same epitaxial layer structure similar photodiodes has been integrated with hybrid optical amplifiers [226]. An improved bandwidth of 16 GHz has been reported for an InGaAs/InP p-i-n photodiode [220, 227]. The 12 μm x 120 μm photodiode with 0.5 μm intrinsic layer thickness was part of a triplexes with different epitaxial layers being bonded on a single Si chip. Using small InP-based membrane p-i-n photodetectors on SOI a bandwidth of 33 GHz was demonstrated by *Binetti* et a1. [228]. In this approach the photodiode structure consisted of an InP membrane input waveguide to couple the light out of a Si photonic wire waveguide into the p-i-n junction, similar to a vertical directional coupler [229].

4.2.2 Performance comparison of silicon photodetector

To enable cost-effective, high-reliability, and mature-manufacturability implementation of short-distance optical interconnect systems, a combination of a silicon photodetector (Si-PD) in the CMOS compatible technology and an 850 nm vertical cavity surface emitting laser (VCSEL) transmitter is a strong motivation for realizing 850 nm optoelectronic integrated circuit (OEIC) receivers based on the existing Si technology. Furthermore, a high-speed CMOS trans-impedance amplifier (TIA) and limiting amplifier (LA) are available and can be monolithically integrated with Si-PD in CMOS compatible process to achieve an all-Si optical receiver [230-235].

There have been several reports on the study of CMOS compatible Si-PD in recent years [236-238]. However, as a common issue, due to the light penetration depth of Si at 850 nm is more than 10 μm [239] as shown in Fig. 4-1. Carriers generated from the bulk Si substrate diffuse slowly and are collected, significantly affecting the response performance and limiting the resulting bandwidth [240-242].

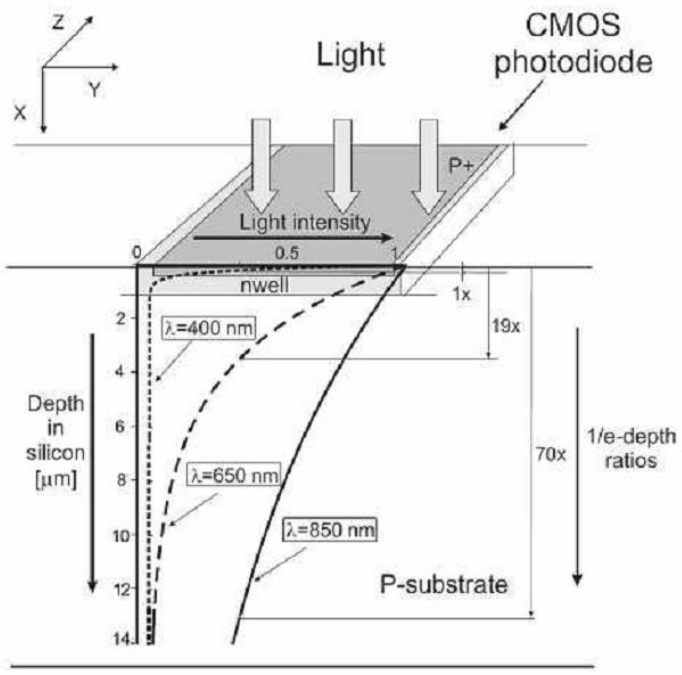


Fig. 4-1 Schematic absorption length of a CMOS-Si-PD and well [239].

Thus, researchers have proposed several methods to increase the speed of CMOS Si-PDs, such as spatially modulated PDs (SM-PDs) [243], as shown in Fig. 4-2; an avalanche photodiode (APD) structure [244-249], as shown in Fig. 4-3; or PDs with a deep n-well (DNW) layer [247-249], as shown in Fig. 4-4; particularly, DNW-PDs with an offset design in terminal electrodes [250], body contact PDs applying an electric filed inside the substrate [251-252], as shown in Fig. 4-5.

However, limited sensitivity of SM-PDs, less effective of APD structure, and incompletely excluded influence of the Si substrate in DNW-PDs are problematic. Recently, silicon-on-insulator (SOI) technology is attracting more attention from both research institutions and industry. Various top silicon layer thicknesses, ranging from a few hundred nanometers to several micrometers, are commercially available. By carefully choosing the SOI substrate, high-speed detectors with reasonable responsivity can be fabricated [253-255], as shown in Fig. 4-6.

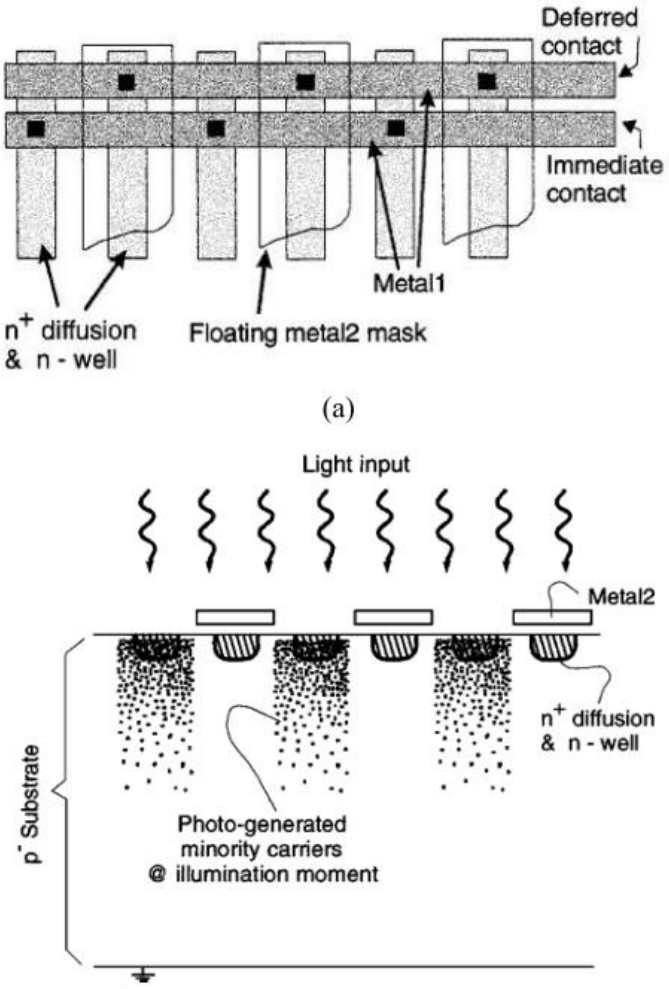


Fig. 4-2 (a) Top view and (b) cross-section of the SM-detector [243].

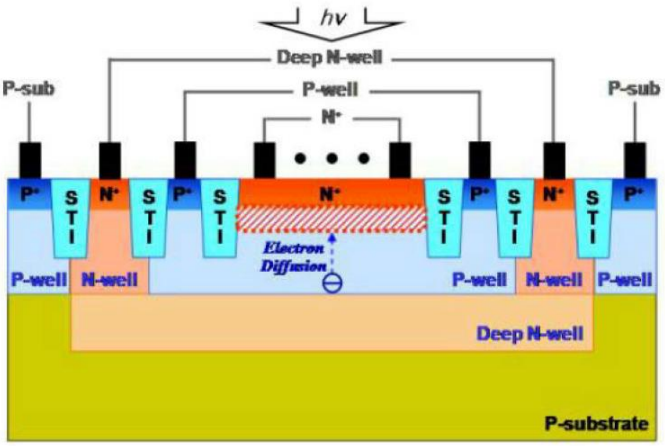


Fig. 4-3 Cross-sectional structures of the CMOS-APD. [245]

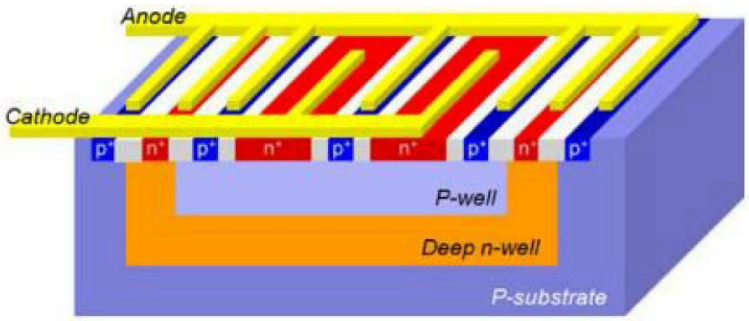


Fig. 4-4 Cross-sectional structures of the CMOS-APD with deep n-well. [248]

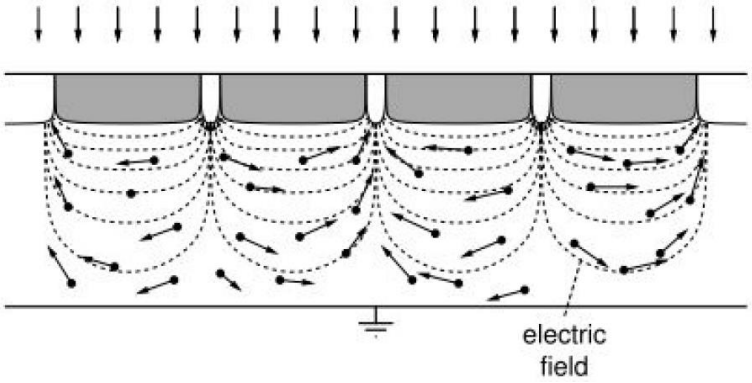


Fig. 4-5 Speed-enhanced photodiode which is obtained by applying an electric field inside the substrate. [251]

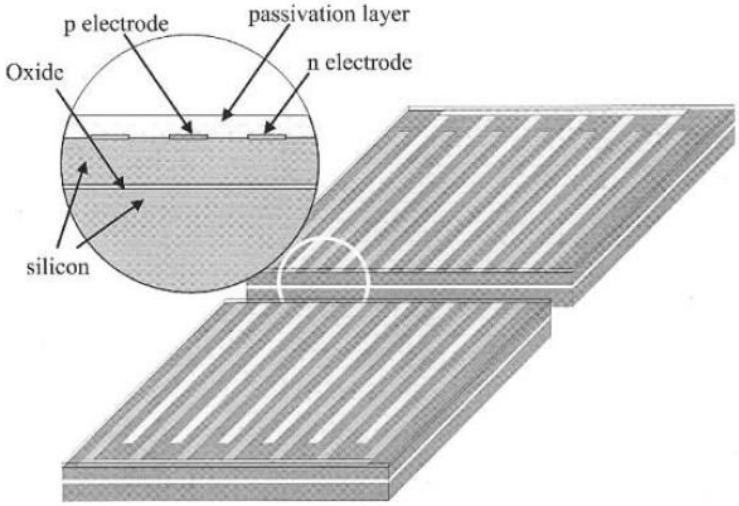


Fig. 4-6 Cross section of the interdigitated lateral p-i-n photodiode on SOI. [254]

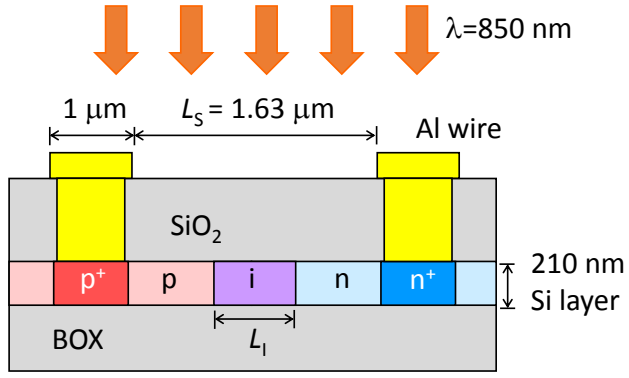
Simultaneously, detectors can be designed in a vertical configuration to improve a bandwidth as mentioned above, but a lateral structure is more preferred as it is suitable for integration of the p-i-n PDs with MOSFETs. The interdigitated configuration of lateral p-i-n PDs can be formed on a low-doped Si substrate [256-258], which is employed to maximize the depleted regions available for high-speed drift carrier collection. However, it increases the diffusion current from the substrate and the parasitic effects due to the diodes in lateral arrangements. Table 4-1 shows a summary of some representative reports on Si-PDs as discussed above, and a comparison with this work.

Table 4-1 Summary of some representative reports on Si-PDs

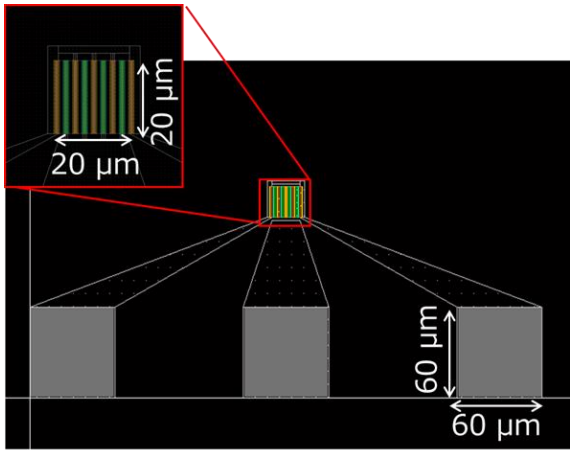
	[235]	[237]	[249]	[258]	[236]	[238]	this work
Process	0.13-μm	epi 0.18-μm	0.18-μm	N.A.	0.13-μm	N.A.	0.18-μm
Type	APD (P^+/N-well)	APD (DNW)	APD (DNW)	Lateral Trench	SOI Lateral	SOI Lateral	SOI Lateral
Thickness (μm)	N.A.	3.8	N.A.	~7	2	2.71	0.21
Finger spacing (μm)	N.A.	2	0.84	3.3	2	2	1.10
Detector area (μm^2)	10×10	70×70	10×10	Ø 75	50×50	50×50	20×20
Bandwidth (GHz)	6.3 @9.9 V	3.1 @15 V	10 @8.3 V	1.5 @3 V(6-dB)	8 @>20 V	3.4 @5 V	13.6 @ 10 V
Responsivity (A/W)	4.67 @10.2 V	0.4 @16.2 V	1.0~ @9 V	0.47 @5 V	0.08 @28 V	0.16 @3 V	0.0075 @10 V
Capacitance (fF)	N.A.	700~	100~150	1040	210	~265	~65
Dark current (nA)	~0.1	~1	~0.05	~0.0015	~1	~0.025	~0.01

4.3 Structure design and fabrication

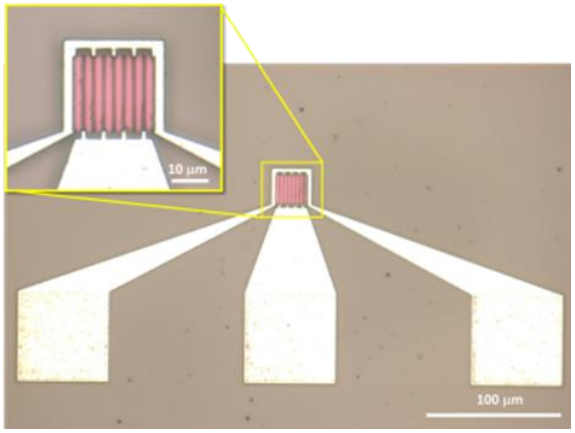
4.3.1 Device structure



(a)



(b)



(b)

Fig. 4-7 (a) Schematic cross-sectional view (b) CAD data and (c) top micrograph view of lateral Si-PIN PDs.

Figure 4-7 (a) shows a schematic cross-sectional view of the lateral Si-PIN PDs fabricated on a SOI substrate, with a 210 nm thick Si absorption layer. A standard model of the SOI lateral Si-PIN PDs was designed with an intrinsic region width (L_i) of 1.09 μm, aluminum electrode with finger width (L_w) of 1 μm and finger spacing (L_s) of 1.63 μm. The CAD data and a top view of the fabricated SOI lateral Si-PIN PDs was shown in Fig. 4-7 (b) and (c). The optical detection area (S_D) and pad size (S_{Pad}) for RF probing are 20 × 20 μm^2 and 60 × 60 μm^2, respectively. The Si layer in the outside of the detection area is etched completely to avoid an excess optical absorption. Doping concentrations of n and p are 3 × 10^{12}/cm^2 and 5 × 10^{12}/cm^2, respectively. Bottom region of the electrode contact, high doping concentrations of n+ and p+ are employed to reduce contact resistance. Doping concentrations of n+ and p+ are both of 4 × 10^{15}/cm^2. In these devices, a lower dark current can be expected because of the very thin Si absorption layer, and a fast response over 10 GHz can be calculated out due to a capacitance smaller than 0.2 pF and the low-speed diffusion current cut-off by the SiO_2 insulation layer. What's more, in order to investigate the frequency response dependence on intrinsic region width (L_i), finger spacing (L_s), detection area (S_D) and pad size (S_{Pad}). Variable elements were designed as shown in Table 4-2.

Table 4-2 Specifications of SOI lateral Si-PIN PDs.

Specification		Standard model
Finger spacing L_s (μm)	0.75, 1.10, 1.63, 2.50, 4.25	1.63
Intrinsic region width L_i (μm)	0, 1/3 L_s, 2/3 L_s, L_s	1.09
Detection area S_D (μm^2)	10 × 10, 20 × 20, 20 × 40, 40 × 20, 30 × 30	20 × 20
Pad electrode size S_{Pad} (μm^2)	30 × 30, 40 × 40, 50 × 50, 60 × 60	60 × 60

4.3.2 CMOS compatible technology and foundry service process

There is another big attraction in silicon photonics, is such available foundry services, especially CMOS foundry having a highly developed process technology [259]. The CMOS foundry service, utilizing the large equipment for electronic circuit fabrication, could produce integrated optical devices on chips. There are some constraints for device design to performance produce, but can be fabricated at a low cost.

In this study, SOI lateral Si-PIN PDs were fabricated through a foundry service and a shuttle process of Institute of Microelectronics in Singapore. Figure 4-8 shows a flow of device fabrication through the foundry service. The concrete layer out and technical details are secret maintenance.

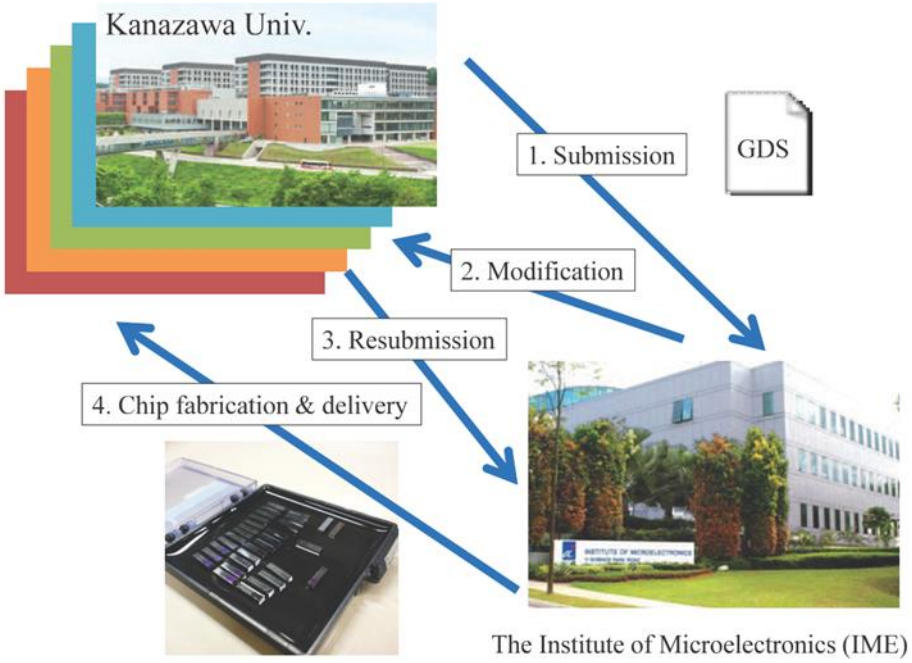


Fig. 4-8 A flow of device fabrication through the foundry service.

4.4 Devices Performance and discussions

4.4.1 Measurement system

Figure 4-9 shows the measurement system and picture for the fabricated SOI lateral Si-PIN PDs. A laser light is normally illuminated on the SOI lateral Si-PIN PDs via an optical fiber for the analyses of static and dynamic characteristics. The core diameter of the optical fiber is 9 μm. A semiconductor laser diode with a center wavelength of 850 nm was employed. When measuring the frequency responses, we used a 10 MHz – 40 GHz network analyzer, and the laser diode was intensity modulated by an electro-optic modulator with a bandwidth of more than 25 GHz. The frequency responses of the modulator and 40 –GHz-RF cables were compensated by using a commercial GaAs PIN-PD with a bandwidth of 30 GHz.

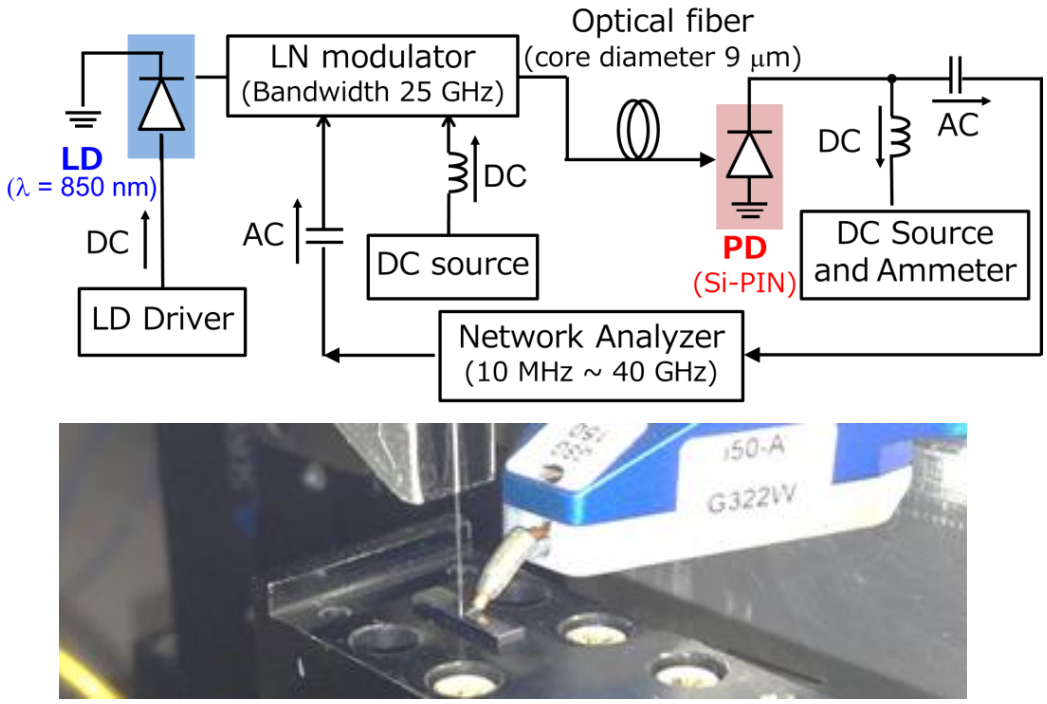
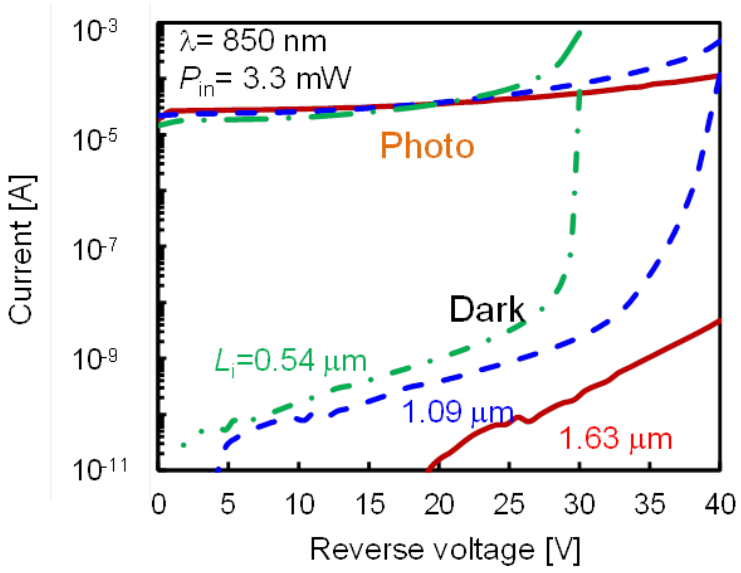


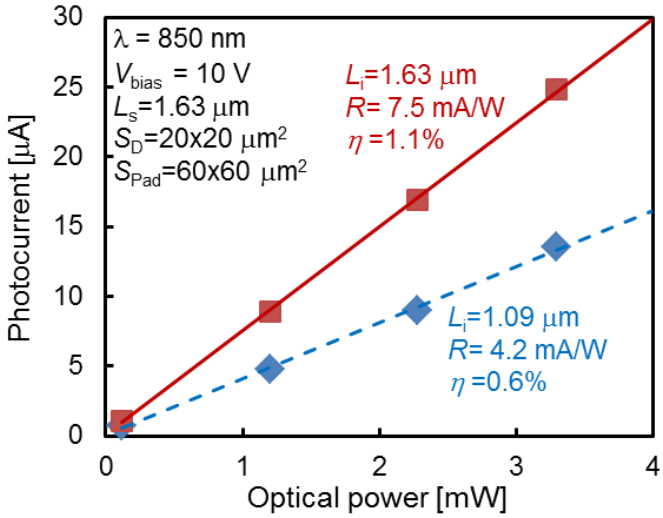
Fig. 4-9 Measurement setup and picture for SOI lateral Si-PIN PDs.

4.4.2 Static characteristics and discussions

SOI lateral Si-PIN PDs were measured in the 0.8 μm wavelength region. Figure 4-10 (a) shows the dark current and photocurrent of current-voltage (I-V) characteristics at various intrinsic region widths. A very low dark current lower than 0.1 nA at a bias voltage below 10 V was obtained. The breakdown voltage was over 40 V at L_i=L_s =1.63 μm, and a better performance of the full-depletion (L_i=L_s) type was demonstrated. The measured responsivity at 850 nm is 7.5 mA/W, corresponding to an external quantum efficiency of 1.1%, as shown in Fig. 4-10 (b).



(a) Dark and photocurrent of current-voltage (I-V) characteristics



(b) Responsivity and external quantum efficiency characteristics

Fig. 4-10 Static characteristics of SOI lateral Si-PIN PDs with various intrinsic region widths at finger spacing of 1.63 μm.

4.4.3 Dynamic characteristics and discussions

Figure 4-11 shows the measured frequency response of the SOI lateral Si-PIN PDs with L_w=1.00 μm, L_i=L_s =1.63 μm, S_D=20 × 20 μm^2, S_{Pad}=30 × 30 μm^2 at a bias voltage of 10 V with a laser light wavelength of 850 nm. The frequency response is normalized at the response of 100 MHz, and a -3 dB bandwidth of 13.6 GHz was obtained.

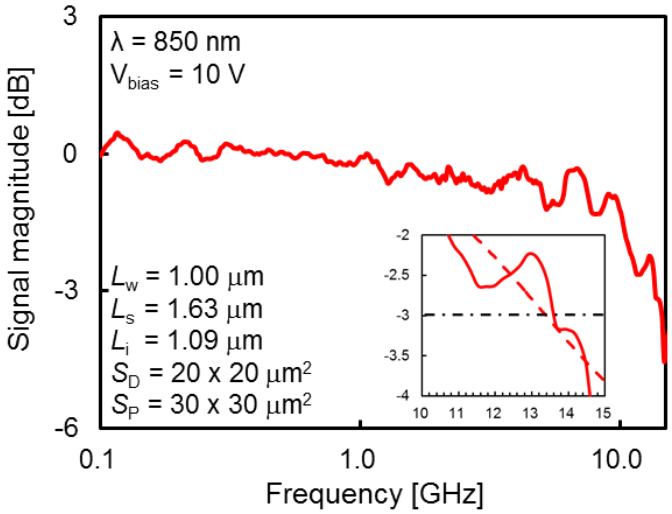


Fig. 4-11 Measured frequency response.

Figure 4-12 shows the voltage dependence of -3 dB bandwidth at various intrinsic region ratios (L_i / L_s) at the finger spacing of 1.63 μm. With increasing of intrinsic region ratio (L_i / L_s), an increase of -3 dB bandwidth was demonstrated. A saturation voltages of approximately 10 V, and the largest -3 dB bandwidth of 12.6 GHz were obtained. Moreover, with a narrower intrinsic region, a rapid saturation trend and a lower -3 dB bandwidth showed a trade-off relationship.

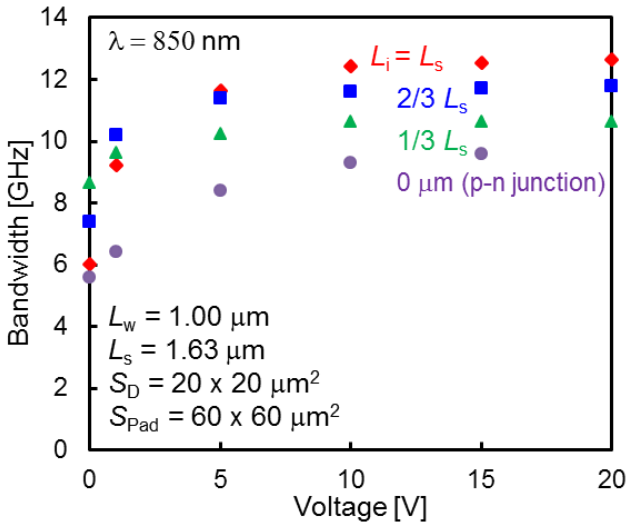


Fig. 4-12 Voltage dependence of bandwidth at various intrinsic region ratios.

In order to investigate the finger spacing dependence of bandwidth in the full-depletion type (L_i=L_s) samples, finger spacings of 0.75, 1.10, 1.63, 2.50, and 4.25 μm were measured at a bias voltage of 10 V. The measurement values are shown in Fig. 4-13 as points (in red). A visible frequency response curve shows an existential optimum design of finger spacing to achieve a maximum bandwidth. This trend is an important feature of SOI lateral Si-PIN PDs. The response time of PDs is primarily limited by two factors: (1) the transit time of photogenerated carriers to the electrode, shown as a dashed line (in green) (the velocity of a hole was fitted to 3.0×10^6 cm/s as a saturation velocity); (2) the total of the depletion region capacitance of the semiconductor (the same as capacitance of the detector area calculated to be about 10^{-14} F) and the capacitance of the pad (a capacitance factor measured to be about 0.045 fF/μm^2), which was estimated and shown as open circles (in blue). An agreement was obtained between the calculated and measurement values. With the miniaturization of finger spacing, a higher frequency response can be supplied because of a shorter drift time. On the other hand, a higher frequency response will be limited by a significant increase in capacitance in a thinner intrinsic region.

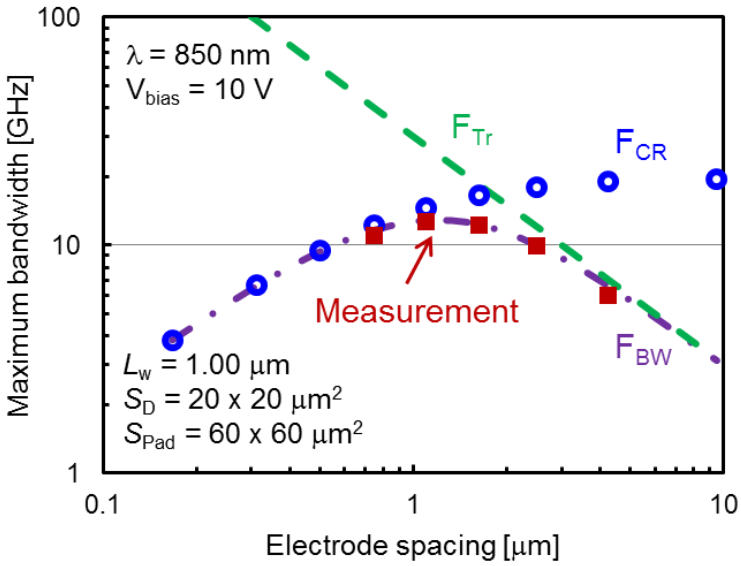
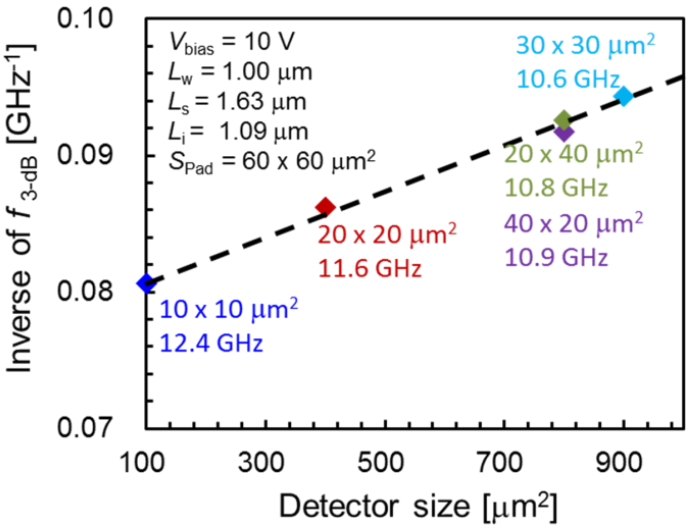
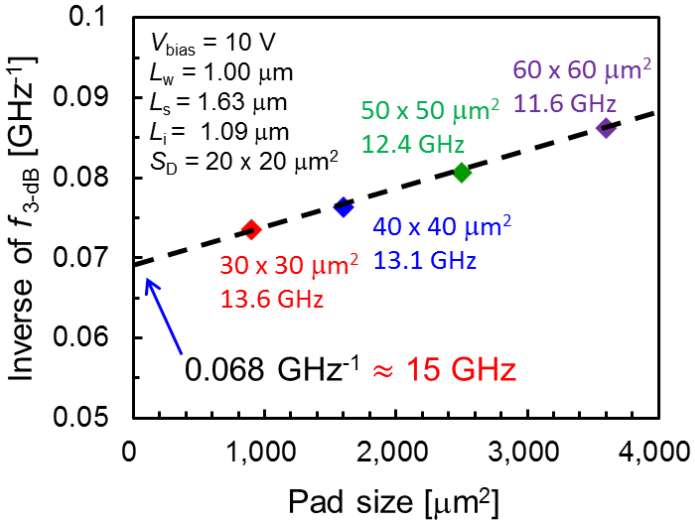


Fig. 4-13 Finger spacing dependence of bandwidth at L_i=L_s.

We also confirmed the detection area (S_D) and pad size (S_{Pad}) dependences of bandwidth as shown in Figs. 4-14 (a) and 4-14 (b). Both show a linear relationship between the inverse of a -3 dB bandwidth and area size, and a -3 dB bandwidth of about 15 GHz was expected without the capacitance of the pad.



(a)



(b)

Fig. 4-14 (a) Detection area dependence and (b) pad size dependence of -3 dB bandwidth.

4.5 Summary and Future works

A lateral thin-film Si-PIN PDs on the SOI substrate was fabricated by a CMOS compatible process. The frequency response dependence of intrinsic width (L_i), finger spacing (L_s), detector area (S_D), and pad size (S_{Pad}) were demonstrated. With the same L_s, a wider L_i shows a larger -3 dB bandwidth, but a slower saturation trend. In the structure of SOI lateral Si-PIN PDs, there is an optimum design of L_s for a maximum bandwidth, because the response time is both limited by the transit time of carriers and the depletion region capacitance of the detector area. A smaller S_D or S_{Pad} causes a linear increase with the inverse of -3 dB bandwidth. The largest -3 dB bandwidth of 13.6 GHz was obtained in device L_w =1.00 μm, L_i =1.09 μm, L_s = 1.63 μm, S_D =20 × 20 μm^2, and S_{Pad} =30 × 30 μm^2, at a reverse bias voltage of 10 V and 850 nm wavelength.

For the future work, a modelling method and optimum design has been carried out and expect to achieve a bandwidth over 40 GHz. In this study, these devices was obtained that can also be operated under 10 V, leading to low power consumption, thus, a silicon receiving, and a photonic integrated circuit of Si_3N_4 waveguide and silicon SOI-PD has been planned. The devices can be expected to realize the optoelectronic integrated circuits (OEIC) on Si-LSIs.

Chapter 5

Conclusions

In order to realize an active optical cable (AOC) interconnection to the LSIs on the Si/SOI substrate, a study on optical integrated circuits of low-loss high-refractive-index waveguide and ultra-high speed Si-PIN photodetector, utilizing a high-efficient directional waveguide grating coupler were carried out.

Firstly, a high-refractive-index (∼2.0) and low-propagation-loss tantalum pentoxide (Ta_2O_5) waveguide was realized. We fabricated Ta_2O_5 strip optical waveguides with a cross section of 400 nm x 10 μm by a chemical solution deposition (CSD) followed by a CF_4 reactive ion etching. The optimum fabrication steps make it possible to obtain the Ta_2O_5 strip optical waveguides with a propagation loss of less than 1 dB/cm at 830 nm, which is significant for optoelectronic integrated circuits in the 0.8 μm wavelength range.

Secondly, a high-efficient directional waveguide grating coupler employing a Ta_2O_5 optical waveguide, which is transparent in 0.8 μm wavelength range was demonstrated. The optical waveguide grating coupler was analyzed by using finite element method (FEM). A coupling efficiency of more than 60% was calculated at the grating period of 530 nm, the duty ratio of 0.50 and the etching depth ratio of more than 0.9 with a thickness of 400 nm. A wavelength dependence of less than 0.65 dB from 800 to 900 nm wavelength was calculated.

Finally, lateral silicon photodetectors fabricated on silicon-on-insulator (SOI) substrate in a complementary metal-oxide-semiconductor (CMOS) compatible process were designed and implemented. In addtion, I discussed structure dependences on the frequency and optimum design for a maximum bandwidth. A standard device fabricated with a 210 nm absorbing layer, a finger width of 1.00 μm, a finger spacing of 1.63 μm, a square detector area of 20 × 20 μm^2, and a pad size of 60 × 60 μm^2 achieved a bandwidth of 12.6 GHz at a bias voltage of 10 V, with a responsivity of 7.5 mA/W at 850 nm wavelength. Photodetector with the same geometry, which was fabricated with a smaller pad size of 30 × 30 μm^2 exhibited a bandwidth of 13.6 GHz.

In a word, these technologies can be expected to realize an OEIC on Si-LSIs in the 0.8 μm wavelength range as a cost-effective implementation.

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Publication List

Journal Papers List

[1] **G. Li**, Y. Hashimoto, T. Maruyama, and K. Iiyama, "High-efficiency Optical Coupling to Planar Photodiode using Metal Reflector loaded Waveguide Grating Coupler," *Opt. Quantum Electron.*, vol. 45, no. 7, pp. 657-663, Jul. 2013.

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[3] **G. Li**, K. Maekita, H. Mitsuno, T. Maruyama, and K. Iiyama, "Over 10 GHz Lateral Silicon Photodetector Fabricated on SOI Substrate by CMOS Compatible Process," *Jpn. J. Appl. Phys.*, vol. 54, no. 4S, pp. 04DG06 (4pages), Mar. 2015.

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[4] **G. Li**, Y. Hashimoto, S. Ebuchi, T. Maruyama, and K. Iiyama, "High-efficiency Optical Coupling to Planar Photodiode using Metal Reflector Loaded Waveguide Grating Coupler," *12th International Conference on Numerical Simulation of Optoelectronic Devices (NUSOD 2012)*, TuB4, Shanghai, China, Aug. 2012.

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Abbreviation List

AOC	active optical cable
a-Si	amorphous Si
AWG	arrayed waveguide gratings
BCB	benzocyclobutene
CAGR	compound annual growth rate
CMOS	complementary metal-oxide-semiconductor
CSD	chemical solution deposition
c-Si	crystalline Si
CVD	chemical vapor deposition
CW	continuous-wave
dB/km	decibels per kilometer
DFB	distributed-feedback
DON	digital optical network
DWDM	dense wavelength-division multiplexing
EDFA	erbium-doped fiber amplifier
EICs	electronic integrated circuit
FEM	finite element method
FTTH	fiber to the home
GaAs	gallium arsenide
Gbps	gigabits per second
Ge	germanium
ICs	integrated circuits
InP	Indium Phosphide
LAN	local area network
$LiNbO_3$	Lithium Niobate
MAN	metropolitan area network
MBE	molecular beam epitaxy
MCVD	modified chemical vapor deposition
MOCVD	metal-organic chemical vapor deposition
MOVPE	metalorganic vapor phase epitaxy
MZI	Mach–Zehnder interferometer
OEIC	optoelectronic integrated circuit
PICs	photonic integrate circuits

p-Si	polycrystalline Si
QCL	quantum cascade laser
QSFP	quad small form factor pluggable
RT	room-temperature
Si	Silicon
SiN_x	silicon nitride
SiO_2	silicon dioxide
SiON	silicon oxynitride
Si-PIN PD	Si-PIN photodetector
SOC	system-on-a-chip
SOI	silicon-on-insulator
SSB	single side band
Ta_2O_5	tantalum pentoxide
TDM	time division multiplexing
ULSI	ultra-large scale integration
VSB	vestigial side band
WDM	wavelength division multiplexing