A study of ultrahigh speed optical integrated circuits on Si substrate

Doctoral dissertation

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Abstract: This study was carried out to realize an active optical cable integrated with Si-LSIs, proposed by the optical integrated circuit of a high refractive index waveguide and an ultra-high speed Si photodetector, utilizing a waveguide grating coupler in the 0.8 μm wavelength range. Firstly, the high refractive index (n ~2.0) and a low propagation loss (< 1 dB/cm) tantalum pentoxide (Ta_2O_5) waveguide with a cross section of 400 nm x 10 μm was realized by a chemical solution deposition followed by a CF_4 reactive ion dry etching. Secondly, a Ta_2O_5 waveguide grating coupler was calculated to achieve a bottom direction coupling efficiency > 60%, with a grating length of 15 μm, at a grating period of 530 nm, a duty ratio of 0.5 and an etching depth ratio > 0.9 with a thickness of 400 nm. Finally, lateral Si-PIN photodetectors fabricated on an SOI substrate by the CMOS compatible process were designed with a finger width of 1.00 μm, a finger spacing of 1.63 μm, a square detector area of 20 × 20 μm^2, and a pad size of 30 × 30 μm^2. A bandwidth of 13.6 GHz was obtained at a bias voltage of 10 V at 850 nm wavelength.

Nowadays, everyone around the world can enjoy themselves by sharing amount of transmitted data, thanks to the large-volume optical fiber transmissions have been widespread in the long-haul communication systems since 1980s. Recently, given a dramatically increasing of the data traffic, at a compound annual growth rate of 40% or even more, in the short-distance communications such as rack-to-rack, board-to-board and chip-to-chip, the optical communications have also been introduced gradually instead of traditional electrical communications, namely, optical interconnections.

Especially, given an integrated circuit of a large-volume optical interface to a high-performance electrical LSI processing is proposed to lead a generational communication system. In order to enable a cost-effective implementation of this optical short-distance connections, a complementary metal-oxide-semiconductor (CMOS) compatible process is an useful, low-cost approach for a monolithic integration of available, complex, and high-speed optical circuits, combining with general 850 nm transmitters and platform Si photodetectors to form an optoelectronic integrated circuit (OEIC) on a Si substrate.

This study was carried out to realize an active optical cable (AOC) integrated with Si-LSIs, proposed by an optical integrated circuit of a low-loss high-refractive-index tantalum pentoxide (Ta_2O_5) waveguide and an ultra-high speed Si-PIN photodetector (Si-PIN PD), utilizing a directional waveguide grating coupler in the 0.8 μm wavelength range. Firstly, the high-refractive-index (n ~2.0) and low propagation loss (< 1 dB/cm) Ta_2O_5 waveguide with a cross section of 400 nm x 10 μm was fabricated by a chemical solution deposition followed by a CF_4 reactive ion dry etching. Secondly, the directional waveguide grating coupler was calculated by using finite element method (FEM) to

achieve a bottom directional coupling efficiency > 60% with a grating length of 15 μm, at a grating period of 530 nm, a duty ratio of 0.5, and an etching depth ratio > 0.9 with a thickness of 400 nm. Finally, the lateral Si-PIN PDs fabricated on an silicon-on-insulator (SOI) substrate (absorber layer thickness of 210 nm) in the CMOS compatible process were designed and implemented with a finger width of 1.00 μm, a finger spacing of 1.63 μm, a square detector area of 20 × 20 μm^2, and a pad size of 30 × 30 μm^2. A bandwidth of 13.6 GHz was obtained at a bias voltage of 10 V at 850 nm wavelength.

In a word, these technologies can be expected to realize an OEIC on Si-LSIs in the 0.8 μm wavelength range as a cost-effective implementation.

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学位論文審査報告書（甲）

１．学位論文題目（外国語の場合は和訳を付けること。）

Study of ultrahigh speed optical integrated circuits on Si substrate

（シリコン基板上超高速光集積回路）

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３．審査結果の要旨（600～650 字）

平成 27 年 1 月 29 日に第 1 回学位論文審査委員会を開催した。平成 27 年 1 月 30 日に口頭発表を実施し、発表終了後に第 2 回学位論文審査委員会を開催した。慎重審議の結果、以下のとおり判定した。なお、口頭発表における質疑を最終試験に代えるものとした。

本論文は、超高速・近距離光インターコネクション用光集積回路のシリコン基板上への実現を目的としている。そして、作製プロセスとして CMOS 互換プロセスを用い、波長 0.8 μm 帯を伝搬波長とすることが特徴である。主な成果は次の 3 つである。まず、SOI（Silicon on insulator）基板を用いた PIN ダイオードを CMOS 互換プロセスのファウンドリーサービスにて作製し、波長 0.8 μm 帯で 10GHz 以上での応答を実現した。また 1 V 程度の低電圧でも高速動作することも明らかにした。次にシリコン基板上に高屈折率酸化物 Ta_2O_5 を用いた導波路幅 10 μm、導波路厚 0.4 μm の光導波路を光露光および CF_4 ガスによる反応性ドライエッチングを用いて作製し、波長 0.8 μm 帯において導波路損失 1dB/cm 以下を得た。さらに、光導波路と光検出器とを高効率結合させる回折格子結合部を有限要素法を用いて設計した。回折格子周期 0.53 μm、デューティ比 0.5、結合長 15 μm において結合効率 60%となることを明らかにした。最後に CMOS 互換プロセスを用いて光導波路（Ta_2O_5 ではなく SiN）と光検出器を集積した光集積回路を作製した。光検出器および光導波路は単体では動作したが、光導波路と光検出器の結合は確認できなかった。

以上の研究成果は、近距離光インターコネクション用のシリコン基板上光集積回路の進展に大きく貢献するものであり、本論文は博士（工学）に値するものと判定した。

４．審査結果　(1) 判　　定（いずれかに○印）　（合　格）・　不合格

(2) 授与学位　　博　士（工　学）