Implementation of Fast, Low Latency 2D IIR Digital filters using Separate Computation of Semizero-State and Zero-Input Responses.

1993 Fiscal Year Final Research Report Summary

Implementation of Fast, Low Latency 2D IIR Digital filters using Separate Computation of Semizero-State and Zero-Input Responses.

Research Project

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Research Category

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Allocation Type

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電子通信系統工学

Research Institution

Kanazawa University

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Keywords

2-D Digital Filter / Image Processing / Multiprocessor / Signal Processor / Block Processing / Ring Connected / State Space Model

Research Abstract

This paper treats multiprocessor implementation of fast, low latency 2D digital filters using block processing. 2D data plane is partitioned into square regions and a ring connected multiprocessor system is used for inter-region parallel processing in vertical direction, each processor filtering each region. Vertical state variables are transfered from a processor to a processor. In a particular region, putting the bottom edge vertical state variables to be zeroes, semizerostate responses of state variables by the left edge horizontal state variables and the input data samples are computed, then complete responses of state variables at the upper and right edges and filter outputs of the region are computed. Computed vertical state variables are transferred from a processor to the next upper processor. The processing progresses in vertical direction, one region at one step. The algorithm results significant decrease in computation amount compared to the conventional block processing algorithm. The system can give high throughput and low latency.
First, the filters expressed by an unity state equation are treated. Inter-region parallel processing is also performed. Computation is load equally allotted to each processor so that the system works in high efficiency. The system was constructed with TI's C-40 signal processor simulator.
Secondly, the filters consisting of cascaded low-order sections are treated. the system has lower computation amount and higher achievable throughput than the former. These are confirmed by simulation using C-40 simulator.

Research Products (4 results)

All Other

All Publications (4 results)

[Publications] 武部 幹: "零状態・零入力応答分離ブロック処理による二次元ディジタルフィルタの実現" 電子情報通信学会技術報告DSP. 92-100. 9-16 (1992)

[Publications] Tsuyoshi Takebe: "Multiprocessor Implementation of 2-D Denominator-Separable Digital Filters Using Block Processing" IEICE Trans.Fundamentals. E75-A. 846-851 (1992)

[Publications] 武部 幹: "ブロック処理縦続型二次元IIRディジタルフィルタのマルチプロセッサ実現" 平成5年度電気関係学会北陸支部連合大会講演論文集. 1. 93 (1993)

[Publications] 武部 幹: "画像処理用縦続形二次元IIRディジタルフィルタの半零状態・零入力応答分離計算による高速実現法" 第16回情報理論とその応用シンポジウム予稿集. 1. 223-226 (1993)

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