Fast Implementation of Two-Dimensional Digital Filter using Block Processing Based on Separate Computation of Zero-State and Zero-Input Responses

1991 Fiscal Year Final Research Report Summary

Fast Implementation of Two-Dimensional Digital Filter using Block Processing Based on Separate Computation of Zero-State and Zero-Input Responses

Research Project

Project/Area Number

02650239

Research Category

Grant-in-Aid for General Scientific Research (C)

Allocation Type

Single-year Grants

Research Field

電子通信系統工学

Research Institution

Kanazawa University

Principal Investigator

TAKEBE Tsuyoshi Kanazawwa University, Faculty of Technology, Department of Electrical and Computer Engineering, Professor, 工学部, 教授 (20019699)

Co-Investigator(Kenkyū-buntansha)

MATSUMOTO Toyoji Kanazawa University, Information Processing Center, Lecturer, 総合情報処理センター, 講師 (20173908)

Project Period (FY)

1990 – 1991

Keywords

Digital Filter / Image Processing / Multi-processor / SIMD Processor / State-Space Model / Moving Picture / Ring Coupled Processors / Block Processing

Research Abstract

Multi-processor implementation of fast two-dimensional digital filters and efficient filtering algorithms are developed. Picture plane is partitioned into blocks of P*Q samples and intra- and inter-block parallel processing s are simultaneously performed. The intra-block processing is based on Roesser's state-space model.
1. Synchronization of inter-block parallel processing.
Bi-directional (horizontal and vertical) and one directional (vertical) ring coupled processing systems are considered. The horizontal and vertical state

variables computed from one block are transferred to the next right and top blocks respectively. Timing condition that each processing system has no waiting to receive state variables is established.
2. Algorithms for intra-block processing.
To increase the processing speed with decreasing of the number of operations per sample and with increasing parallel computation degree, zero-state and quasi zero-state block processing methods are proposed and compared with block processing method. Qusai block method is found to be superior to others.
3. Efficient processing system for denominator separable transfer function.
As the block state matrix of the filter has high sparsity, the rows and columns are interchanged respectively to reduce the matrix size. as a result, some raising of the throughput of the system and some reduction of the number of required processors are achieved.
4. Optimum design of one directional ring coupled system.
One directional system has advantage of lower frame latency than bi-directional system, where frame latency is defined as the time from beginning to the end of one frame processing. Optimum design conditions of the system to realize assigned throughput using minimum number of processors , i. e., the form and size of a block, number of simultaneously processed blocks, are found by computer simulation.

Research Products (12 results)

All | Other

All | Publications (12 results)

[Publications] 武部 幹,平野 泰宏,村上 雅俊,橋本 芳文: "2次元IIRディジタルフィルタのマルチプロセッサ実現法" 電子情報通信学会技術報告DSP. 90ー4. 25-32 (1990)

[Publications] 武部 幹,平野 泰宏,村上 雅俊,橋本 芳文: "マルチプロセッサによる高速2次元IIRディジタルフィルタの実現" 電子情報通信学会技術報告DSP. 90ー77. 15-22 (1990)

[Publications] 武部 幹,平野 泰宏,村上 雅俊: "複数のマルチPEチップを用いた2次元IIRディジタルフィルタのSIMD実現" 電子情報通信学会第5回デイジタル信号処理シンポジウム論文書. Bー3ー1. 1-8 (1990)

[Publications] Tsuyoshi Takabe,Masatoshi Murakami and Koji Hatanaka: "Microprocessor Implementation of 2-D Denominator-Separable Digital Filters" Digest of Ninth Kobe International Symposium on Electronics and Information sciences. 37-1-37-9 (1991)

[Publications] 橋本 芳文,武部 幹: "2次元IIRディジタルフィルタの並列実現法(領域間並列処理に基づく実現)" 平成3年度電気関係学会北陸支部連合大会構演文集. 240-241 (1991)

[Publications] 橋本 芳文,武部 幹: "一方向リング結合マルチプロセッサによる2次元IIRディジタルフィルタの実現" 電子情報通信学会第6回ディジタル信号処理シンポジウム論文集. A2ー1. 49-54 (1991)

[Publications] Tsuyoshi Takebe, Yasuhiro Hirano, Masatoshi Murakami and Yoshibumi Hashimoto: ""Multi-Processor Implementation of Two-Dimensional IIR Digital Filters"" Tech. Rep. of IEICE Japan. DSP90-4. 25-32 (1990)

[Publications] Tsuyoshi Takebe, Yasuhiro Hirano, Masatoshi Murakami and Yoshibumi Hashimoto: ""Fast Multi-Processor Implementation of Two-Dimensional IIR Digital Filters"" Tech. Rep. of IEICE Japan. DSP90-77. 15-22 (1990)

[Publications] Tsuyoshi Takebe, Yasuhiro Hirano, Mastoshi Murakami: ""SIMD Implementation of Two-Dimensional IIR Digital Filters using Multi PE Chips"" Proc. on IEICE 5th DSP Symposium. B-3-1. 1-8 (1990)

[Publications] Tsuyoshi Takebe, Masatoshi Murakami and Koji Hatanaka: ""Microprocessor Implementation of 2-D Denominator-Separable Digital Filters"" Digest of Ninth Kobe Intern. Symp. on Electronics and Information Sciences. 37-1-9 (1991)

[Publications] Hashimoto Yoshibumi and Tsuyoshi Takebe: ""Parallel Implementation of Two-Dimensional Digital Filters-Based on Inter-Block Parallel Processing"" Proc. of Hokuriku District Joint Symp. of Inst's of Electrical Engineers. 240-241 (1991)

[Publications] Yoshibumi Hashimoto and Tsuyoshi Takebe: ""Multi-Processor Implementation of Two-Dimensional IIR Digital Filter using One Directional Ring Connection"" Proc. on IEICE 6th DSP Symposium. A2-1. 49-54 (1991)

URL: https://kaken.nii.ac.jp/report/KAKENHI-PROJECT-02650239/026502391991kenkyu_seika_hokoku_

Published: 1993-03-15