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Charge Trapping Characteristics of Al_2O_3/Al-rich Al_2O_3/SiO_2 Stacked Films Fabricated by Radio-Frequency Magnetron Co-Sputtering

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A thin-film structure comprising Al_2O_3/Al-rich Al_2O_3/SiO_2 was fabricated on Si substrate. We used radio-frequency magnetron co-sputtering with Al metal plates set on an Al_2O_3 target to fabricate the Al-rich Al_2O_3 thin film, which is used as a charge storage layer for nonvolatile Al_2O_3 memory. We investigated the charge trapping characteristics of the film. When the applied voltage between the gate and the substrate is increased, the hysteresis window of capacitance-voltage (C-V) characteristics becomes larger, which is caused by the charge trapping in the film. For a fabricated Al-O capacitor structure, we clarified experimentally that the maximum capacitance in the C-V hysteresis agrees well with the series capacitance of insulators and that the minimum capacitance agrees well with the series capacitance of the semiconductor depletion layer and stacked insulator. When the Al content in the Al-rich Al_2O_3 is increased, a large charge trap density is obtained. When the Al content in the Al-O is changed from 40 to 58 %, the charge trap density increases from 0 to $18\times10^{18}\,\mathrm{cm}^{-3}$, which is 2.6 times larger than that of the trap memory using SiN as the charge storage layer. The device structure would be promising for low-cost nonvolatile memory.

Key words: radio-frequency magnetron sputtering, oxide, Al-rich Al_2O_3/SiO_2 interface, charge trap, C-V hysteresis, MIS theory

1. Introduction

Nanoscale devices have been widely studied [1-5] for large-scale integration. In particular, TaN-Al_2O_3-SiN-oxide-silicon trap memory devices [3-5] have been attracting increasing attention because they are expected to offer extremely large-scale integration due to their thin tunnel insulator (SiO_2) and thin block insulator (Al_2O_3).

Recently, we proposed a simplified trap memory that uses Al_2O_3 for the tunnelling insulator and blocking insulator and Al-rich Al_2O_3 for the charge storage layer. We clarified that the structure is very effective for nanoscale devices due to its simple structure and thin insulator [6-9]. However, a concern for this device is the interface between the Al_2O_3 and Si. It has been reported that defects near the interface degrade the mobility in field-effect transistors considerably [10,11]. The low mobility causes low operation speed, which is 1/10 that of the conventional value.

In the present work, to resolve the above concern, we fabricated an Al_2O_3/Al-rich Al_2O_3/SiO_2/Si structure using the radio-frequency (RF) magnetron co-sputtering method. The structure has three merits. The first is that SiO_2 is already very widely used as the tunnelling insulator in conventional nonvolatile memory [12] so that its use in the memory device enables us to use the prevailing process, i.e., thermal oxidation. The second is an ideal SiO_2/Si interface, near which there are almost no defects so that the mobility degradation does not occur. The third is that the Al-rich Al_2O_3 layer can produce many trap sites as pointed out previously [6-9].

For the Al_2O_3/Al-rich Al_2O_3/SiO_2/Si structure, capacitance evaluation, or in other words, dielectric constant evaluation, is very important for investigating the electrical field across each layer, which is useful for analyzing band bending when programming and erasing. For the capacitance evaluation, orthodox MIS (metal-insulator-semiconductor) theory would be effective. In this article, we calculate the

insulator capacitance of each stacked film and the semiconductor depletion-layer capacitance theoretically. Using these values, we estimate the maximum and minimum capacitance in capacitance-voltage (C-V) hysteresis curves. The estimated values agree well with the experimental ones. From this analysis, the capacitance value in each layer is confirmed.

In the Al-rich Al_2O_3 layer, how the charge trap density changes as a function of the Al content is still not fully understood. Therefore, we changed the Al content from 40 to 60 % and evaluated the charge trap density. We also examined the data retention of the film.

The rest of this paper is organized as follow. Section 2 presents experimental procedures for the film. Section 3 describes the experimental results, which includes the film deposition characteristics (the Al content and leakage current density), C-V characteristics, charge trap density, and data retention. Conclusions are finally described in Section 4.

2. Experiment

In this experiment, we used (100) n-type Si wafers ($\rho \cong 1.5\times10^{-2}$ Ω cm,) as substrates. As shown in Fig. 1(a), 2.0 nm of SiO_2 was first formed as a tunnel barrier insulator by thermal oxidation. Next, 5.4 nm of Al-rich Al_2O_3 was deposited as a charge storage layer by the co-sputtering method. Finally, 7.3 nm of stoichiometric Al_2O_3 was deposited as the blocking barrier insulator by conventional RF sputtering. The sample was annealed at 200 ^{o}C for 1 hour effectively during deposition because the substrate temperature was set at 200 ^{o}C. In this experiment, annealing at 550 ^{o}C as in ref. 9 was not performed after the Al_2O_3 blocking layer was deposited. A gate electrode with a diameter of 100 μm was formed by thermal evaporation of Al. The

band diagram of this structure is shown in Fig. 1(b). Al_2O_3 has a 2.8-eV conduction barrier height [13]. In Al-rich Al_2O_3, the localized level is thought to be about 2.4 eV from the conduction band [14]. Regarding conduction band offsets, the band diagram in Fig. 1(b) is not accepted universally. There is an experimental report that shows much lower values in the case of an ultrathin layer [15]. The conduction band offsets of the ultrathin layer is an important issue. Much research will be necessary to clarify this point.

Here, we explain the co-sputtering method. For the fabrication of Al-rich Al_2O_3, we used RF magnetron co-sputtering equipment [9]. During co-sputtering, Al metal plates (plate size: 2 cm×0.5 cm) were set on the Al_2O_3 target, which had a diameter of 9.2 cm. The Al content of the Al-O film can be controlled by changing the areal ratio of the Al metal on the target. A schematic representation of the co-sputtering system is shown in Fig. 2, where (a) and (b) are cross-sectional and top views, respectively. Atoms are sputtered from a target and reach wafers as shown in Fig. 2(a). The ratio of sputtered atoms from the target is determined by the ratio of Al plate area in the erosion region area in Fig. 2(b).

During deposition of Al_2O_3 and Al-rich Al_2O_3, Ar gas was used for sputtering. RF frequency was 13.56 MHz. The distance between the target electrode and substrate electrode was about 4 cm. After deposition, the deposited film thickness was measured with a spectroscopic ellipsometer. To investigate the Al content in the Al-O film, we used an electron probe micro-analyzer, which allows us to evaluate the Al content non-destructively by radiating an electron beam to the sample. Acceleration voltage and sample current were 15 kV and 20 nA, respectively. Beam size was 30 μm.

Electrical measurements were performed using a probe at room temperature.

Leakage current was measured with a precision semiconductor parameter analyzer (HP4156). Capacitance was measured with a precision LCR meter (HP4284A) at 1 MHz.

3. Results and Discussion

3.1. Film deposition

First, we describe the deposition characteristics of RF-magnetron co-sputtering. Figure 3(a) shows the Al content in the Al-rich Al_2O_3 as a function of the areal ratio of Al metal on the Al_2O_3 target. A ratio of zero means there are no Al metal plates on the target, which corresponds to the deposition of stoichiometric Al_2O_3. A ratio of 100 % means the Al_2O_3 target is completely covered with Al plates. It is clear that the Al content changes linearly as a function of the areal ratio. In the experiment, the Al content reached as high as 70 %, which can provide sufficiently Al-rich Al_2O_3.

The leakage current characteristics of the structure in Fig. 1 with an Al content of around 50 % are shown in Fig. 3(b). When the electric field is smaller than 2×10^8 V/m, leakage current is on the order of 10^{-9} A/cm^2, which is almost the same level as that for Al-O fabricated by electron-cyclotron-resonance sputtering [16] and in our previous work [9].

3.2. Capacitance-voltage characteristic

Here, we first discuss the C-V characteristic of the single Al-rich Al_2O_3 layer with an Al content 50 % to investigate the permittivity. The sample was deposited on (100) n-type Si wafers ($\rho \cong 5\ \Omega$ cm,) as substrates. The film thickness was 76 nm. Annealing was not performed after deposition. A gate electrode with a diameter of 200 μm was formed by thermal evaporation of Al.

We measured the high-frequency C-V characteristics at 1 MHz at room temperature. The sweep rate was about 1 V/sec. The result is shown in Fig. 4. The voltage to the gate electrode was swept from 7 to -7 V. Next, the voltage was reversed from -7 to 7 V. Arrows in Fig. 4 show the C-V hysteresis direction.

Next, we discuss the capacitance value in Fig. 4 using MIS theory. When the maximum applied gate voltage is 7 V, the capacitance value is almost equal to insulator capacitance C_i. From Fig. 4, C_i is estimated to be about 30 pF. The C_i is the capacitance of Al-rich Al_2O_3. Here, we consider the dielectric constant of the insulator. Using the relation $C=\varepsilon S/d$ and the vacuum permittivity of 8.85×10^{-12} F/m, we estimate the dielectric constant to be 8.2. From previous research [17], it is known that the dielectric constant of stoichiometric Al_2O_3 is 8.1. Then, the dielectric constant of Al-rich Al_2O_3 with Al content of 50 % is almost the same as that of stoichiometric Al_2O_3. Therefore, for easy calculation, we set the dielectric constant of stoichiometric Al_2O_3 and Al-rich Al_2O_3 with Al content of 50 % to be 8.

Next, we consider the minimum capacitance C_{min} when V=-7 V. The C_{min} is the series capacitance of C_i and the semiconductor depletion-layer capacitance C_D (i.e., $1/C_{min} = 1/C_i + 1/C_D$). The depletion layer width of semiconductor W is calculated by the formula [18]

$$W^2 = 4\varepsilon_{Si}kT/(q^2 N_D)\cdot\ln(N_D/n_i), \quad (1)$$

where ε_{Si} is the permittivity of Si, k is the Boltzmann constant, T is temperature, q is the elementary charge, N_D is the impurity concentration, and n_i is the intrinsic carrier density. Using the resistivity of the wafer ($\rho\approx$ 5 Ωcm), we estimate N_D to be 1×10^{15} cm^{-3} [18]. Using $n_i=1.45\times10^{10}$ cm^{-3}, we have

$$\ln(N_D/n_i) = 11.1 \ . \quad (2)$$

Then, using T=20 ^{o}C, q= 1.6×10^{-19} C, and ε_{Si} =$11.9\times8.85\times10^{-12}$ F/m, we can estimate W to be 860 nm. Then, we have

$$C_D = \frac{\varepsilon_{Si}}{W}\cdot\pi(100\mu m)^2 = 3.8 \text{ pF} . \quad (3)$$

Using C_i and C_D, we can estimate C_{min} as 3.4 pF. This value is very close to the experimental value of 3 pF.

Next, we measured the high-frequency C-V characteristics of the Al-rich Al_2O_3 structure in Fig. 1 with an Al content of 50 % at 1 MHz at room temperature. The sweep rate was about 1 V/sec. The results are shown in Fig. 5. The maximum applied gate voltage was 1, 2, 3, 4, or 5 V. When the maximum applied gate voltage was 1 V, the voltage to the gate electrode was swept from 1 to -1 V. Next, the voltage was reversed from -1 to 1 V. We repeated this process with maximum applied gate voltages from 2 to 5 V. The hysteresis voltage window ΔV (the difference voltage between the hysteresis at mid capacitance in C-V curves, i.e., 26pF) becomes large when the maximum applied gate voltage increases. Arrows in Fig. 5 show the C-V hysteresis direction. From this characteristic, we know that electrons or holes tunnel through the SiO_2.

Figure 6(a) shows the ΔV-ΔC plot when the maximum applied gate voltage is changed, where the ΔC is the difference between the large and small capacitances at the gate voltage of 0V in Fig. 5. It is clear that ΔV and ΔC become larger when the maximum applied gate voltage increases.

Figure 6(b) shows ΔV as a function of the maximum applied gate voltage. The ΔV does not increase linearly. It is almost zero when the maximum applied gate voltage is around 0 V. When the maximum applied gate voltage increases, ΔV increases rapidly. This is the same as in our previous work [8].

Next, we discuss the capacitance value in Fig. 5 using MIS theory. When the maximum applied gate voltage is 5 V, the capacitance value is almost equal to insulator capacitance C_i. From Fig. 5, C_i is estimated to be about 35 pF. The C_i is equal to the series capacitance of SiO_2, Al-rich Al_2O_3, and Al_2O_3 (i.e., $1/C_i = 1/C_{SiO_2} + 1/C_{Al-O} + 1/C_{Al_2O_3}$, where C_{SiO_2} , C_{Al-O} , and $C_{Al_2O_3}$ are the capacitances of SiO_2, Al-rich Al_2O_3, and Al_2O_3, respectively. The dielectric constants of SiO_2 and Al_2O_3 are 3.9 and 8, respectively. The dielectric constant of Al-rich Al_2O_3 with Al content of 50% is 8 as discussed above. Then, we can estimate C_{SiO_2} as

$$C_{SiO_2} = \frac{3.9 \times 8.85 \times 10^{-12} \text{ F/m}}{2.0 \text{ nm}} \cdot \pi(50\mu m)^2 = 135 \text{ pF} . \quad (4)$$

Similarly, we can estimate C_{Al-O} and $C_{Al_2O_3}$ as 103 and 76.1 pF, respectively. Therefore, insulator capacitance C_i is estimated as

$$C_i = \frac{1}{1/C_{SiO_2} + 1/C_{Al-O} + 1/C_{Al_2O_3}} = 33.1 \text{ pF} . \quad (5)$$

This value is consistent with the experimental results.

Next, we consider the minimum capacitance C_{min} when V=-5 V. The C_{min} is the series capacitance of C_i and the semiconductor depletion-layer capacitance C_D. The depletion layer width of semiconductor W is calculated by formula (1). Using the resistivity of the wafer ($\rho \cong 1.5 \times 10^{-2}\ \Omega$ cm), we estimated N_D to be $2 \times 10^{18}\ \text{cm}^{-3}$ [18]. Using $n_i = 1.45 \times 10^{10}\ \text{cm}^{-3}$, we have

$$\ln(N_D / n_i) = 18.7 . \quad (6)$$

Then, using the same parameters T, q, and ε_{Si}, we can estimate W to be 25 nm. Then, we have

$$C_D = \frac{\varepsilon_{Si}}{W} \cdot \pi(50\mu m)^2 = 33.1 \text{ pF} . \quad (7)$$

Using C_i and C_D, we can estimate C_{min} as 16.6 pF. This value is very close to the experimental value of 17 pF.

Therefore, in the fabricated stacked thin film, it is clarified that the dielectric constant of SiO_2 is 3.9 and that of stoichiometric Al_2O_3 and Al-rich Al_2O_3 with Al content of 50 % is 8.

3.3. Charge trap density

Next, we discuss the charge trap density in the Al-rich Al_2O_3 film. The stored charge per unit area ΔQ can be evaluated as $\Delta Q = C_b \Delta V/2$, where C_b is the capacitance per unit area of the blocking barrier insulator [19]. The C_b is written as $C_b = \varepsilon / d_b$, where d_b is the blocking insulator's thickness and ε is its permittivity. Then, we can estimate d_b as 7.3+5.4/2=10 nm. The ε is $8 \times 8.85 \times 10^{-12}$ F/m. Then, C_b is estimated to be 7.08×10^{-3} F$\cdot$m^{-2}. Since ΔV is 2.9 V when the maximum applied gate voltage is 5 V, ΔQ of the Al-rich Al_2O_3 memory is estimated to be 10.3×10^{-7} C$\cdot$cm^{-2}, so that the electron trap density [$N_e = \Delta Q/(5.4\text{nm} \times 1.6 \times 10^{-19} C)$] is estimated to be 11.9×10^{18} cm^{-3}. This value is larger than that of metal-nitride-oxide-silicon, which is 7×10^{18}[cm^{-3}] [19].

Next, we investigate the charge trap density as a function of Al content. The results are shown in Fig. 7. In the experiment, the gate voltage of 5 or -5 V was applied for 1 sec. The charge trap density is almost 0 when Al content is 40 % (stoichiometric Al_2O_3). When Al content increases, the charge trap density increases. When the Al content is 58 %, the charge trap density reaches 18×10^{18} cm^{-3}. This

value is larger than the previous values ($8.1\times10^{18}\,cm^{-3}$ in ref. 7 and $14.4\times10^{18}\,cm^{-3}$ in ref. 8). It is expected that the more the Al content increases, the larger the charge trap density becomes. When memory cell size is 10-nm square and the charge trap layer is 2-nm thick, we estimate the number of trapped electrons to be 3.6 using the charge trap density of $18\times10^{18}\,cm^{-3}$. In the conventional silicon-oxide-nitride-oxide-silicon trap memory, the average number of trapped electrons is estimated to be only 1.4 by using the charge trap density of $7\times10^{18}\,cm^{-3}$. Moreover, due to the statistical fluctuation, traps can not exist in many cells. However, with Al-rich Al_2O_3, we can easily realize the situation with many trap sites because Al-rich Al_2O_3 maintains its nonstoichiometric characteristic even at the atomic level (1-nm order). The total change in the number of electrons in the Al-rich Al_2O_3 layer during injection and ejection is 7.2, which corresponds to the change of not $\Delta V/2$ but of ΔV. This value is consistent with that in the previous consideration [7].

3.4. Data Retention

Finally, we measured the data retention. The measurement temperature was 20 ^oC. The data retention for the samples with Al content of 50 % is shown in Fig. 8. First, we applied 5 V to the gate for 1 sec and measured the capacitance value as a function of time under gate voltage of 0 V (H in Fig. 8). After measuring H data, we applied -5 V to the gate for 1 sec and measured it again under gate voltage of 0 V (L in Fig. 8). The capacitance value changes gradually because the thickness of SiO_2 is comparatively small (2 nm). However, if the thickness increases by 1 nm, the leakage current would decrease to 1/1000 so that the slope of the capacitance change would decrease to 1/1000 [10,11]. Therefore, it is expected that the device could store data for more than $3x10^8$ s by increasing the thickness of SiO_2 to 3 nm.

Figure 9 shows the data retention for the samples with Al content of 58 %. In this case, the retention characteristic is not better than that in Fig. 8. For this sample, the thickness of SiO_2 should be increased to 4 nm, an increase of 1 nm from 3 nm. By increasing SiO_2 thickness, it is also expected that the sample with Al content of 58 % could store data for more than $3x10^8$ s. A stacked structure with 4-nm-thick SiO_2, 2-nm-thick Al-rich Al_2O_3, and 10-nm-thick Al_2O_3 could be fabricated from the viewpoint of aspect ratio even when the memory cell size is 10-nm square.

4. Conclusion

In summary, we fabricated Al_2O_3/Al-rich Al_2O_3/SiO_2 thin film using thermal oxidation and RF magnetron co-sputtering. We clarified experimentally that the maximum capacitance in the C-V hysteresis agrees well with the series capacitance of insulators and that the minimum capacitance agrees well with the series capacitance of the semiconductor depletion layer and stacked insulator. When the Al content in the Al-rich Al_2O_3 is increased, a large charge trap density is achieved; it is 2.6 times larger than that of the conventional trap memory. The proposed fabrication method uses only two elements (Al and O atoms) on the tunnelling insulator (SiO_2), which might be suitable for fabricating nanostructures because of the simple gate structure. Moreover, the bit cost for memory devices made in this way might be very low compared with other methods because only Al and O atoms need to be prepared. The device structure would be promising for low-cost nonvolatile memory.

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Figure captions:

Fig. 1. Memory structure fabricated by RF magnetron co-sputtering: (a) Cross section and (b) energy band diagram.

Fig. 2. RF magnetron co-sputtering method: (a) Cross-sectional view and (b) top view.

Fig. 3. Characteristics of the Al-rich Al_2O_3 sample: (a) Al content as a function of the areal ratio of Al metals on Al_2O_3 target and (b) leakage current density of the fabricated sample with Al content of 50%.

Fig. 4. C-V characteristics of the single Al-rich Al_2O_3 layer with Al content of 50%.

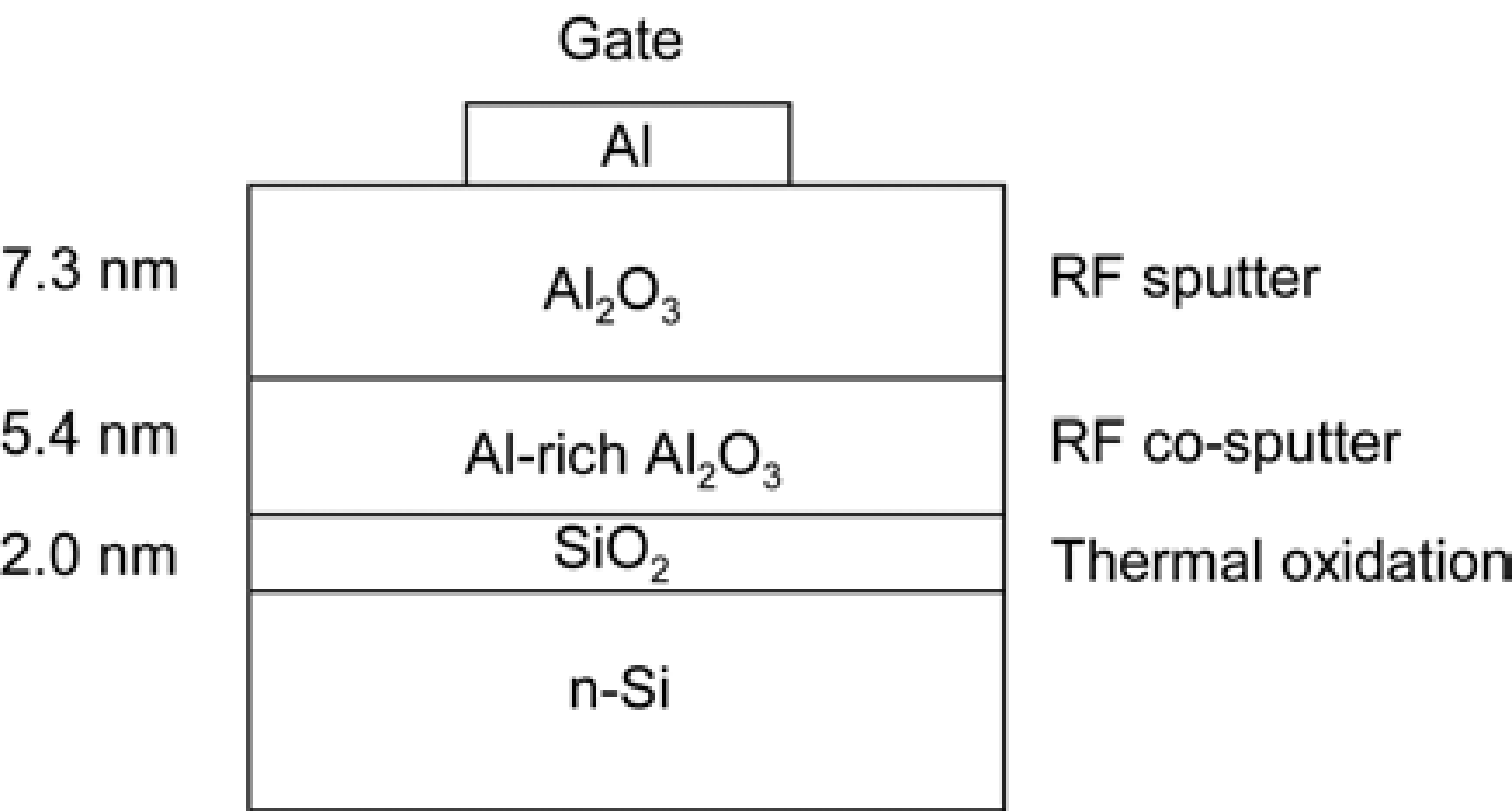
Fig. 5. C-V characteristics of the sample in Fig. 1 with Al content of 50%.

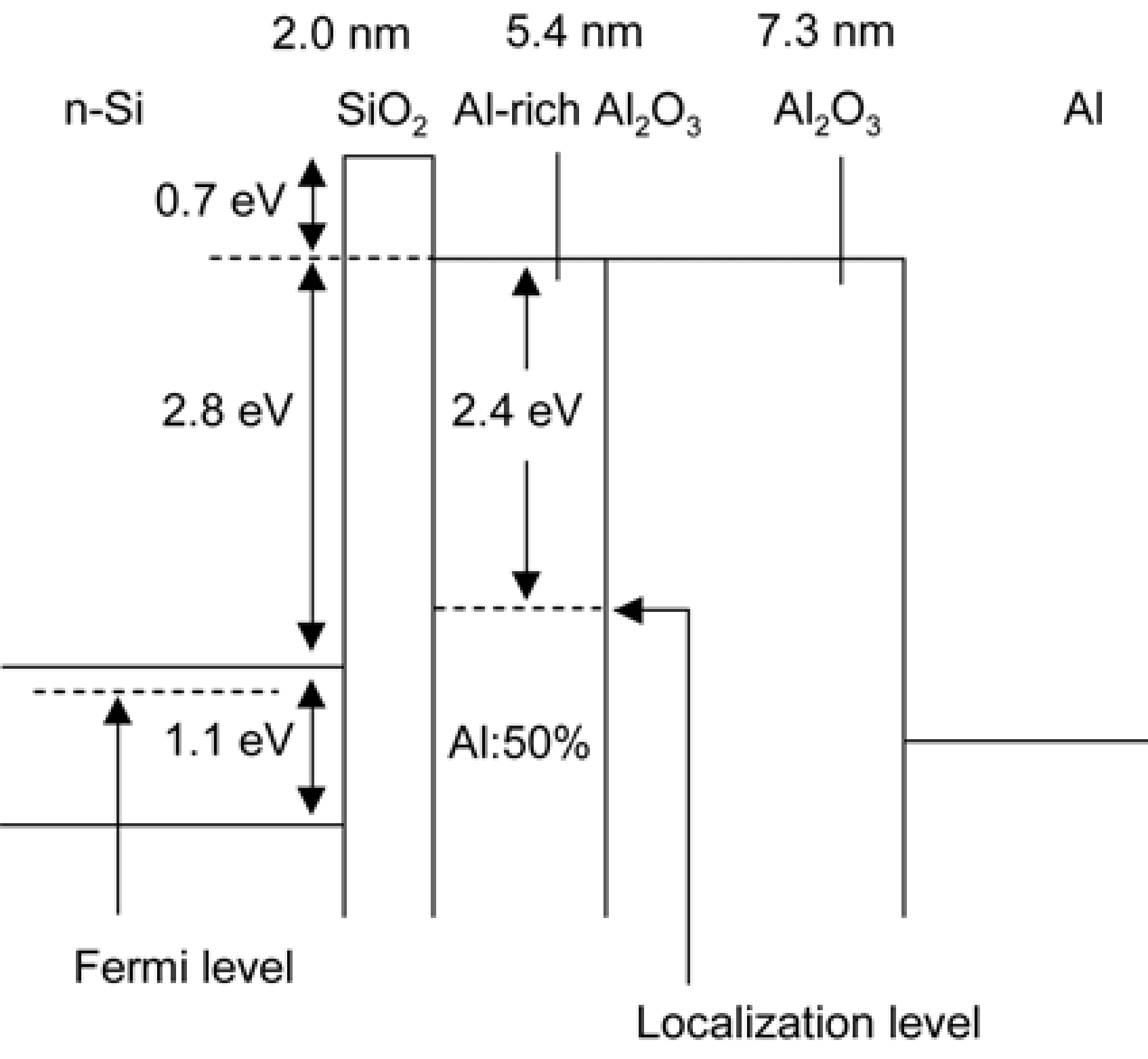
Fig. 6. Hysteresis window in voltage ΔV as a function of (a) the hysteresis window in capacitance ΔC and (b) the maximum applied gate voltage for the sample in Fig. 1 with Al content of 50 %.

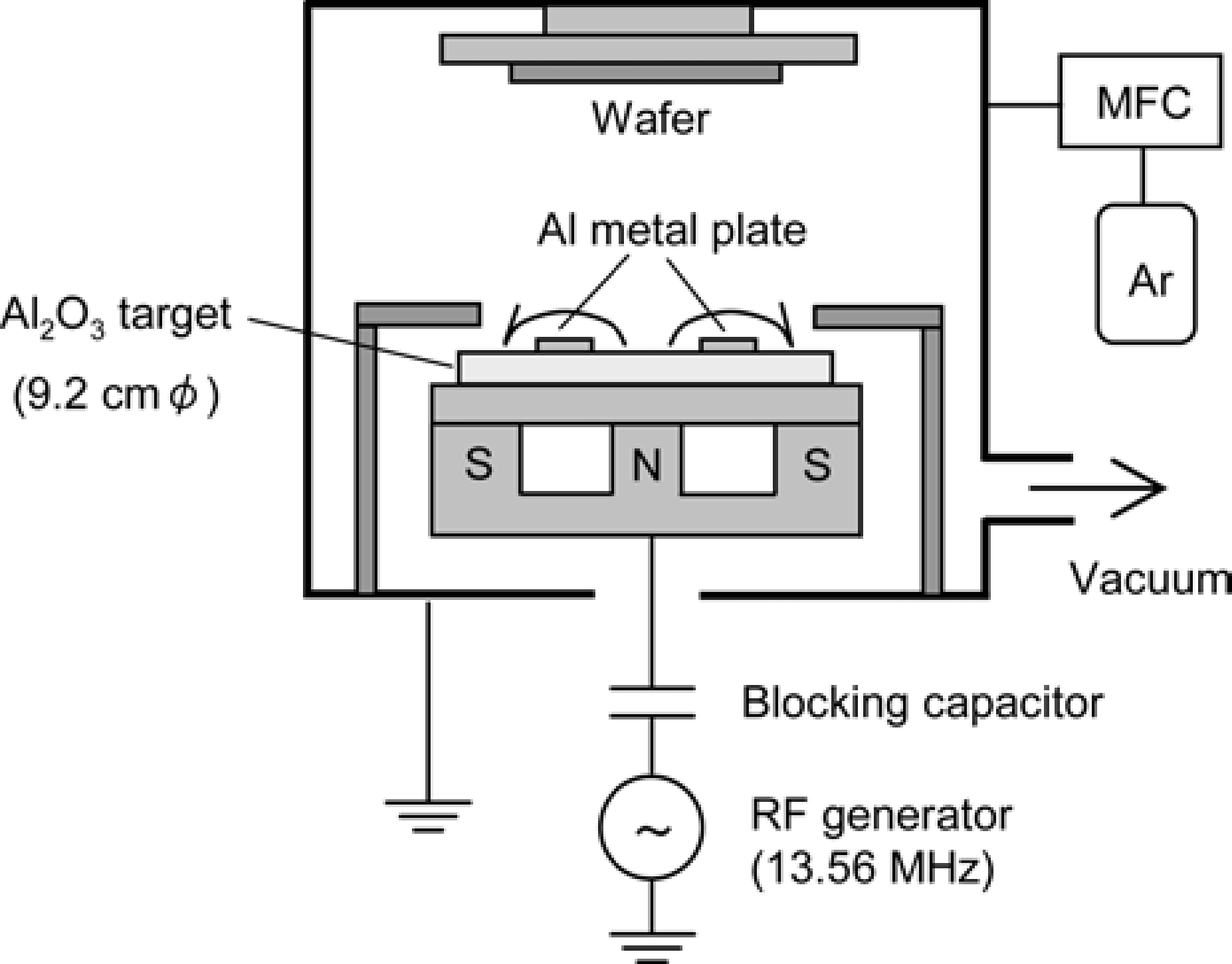
Fig. 7. Charge trap density as a function of Al content for samples with various Al-rich Al_2O_3 layers.

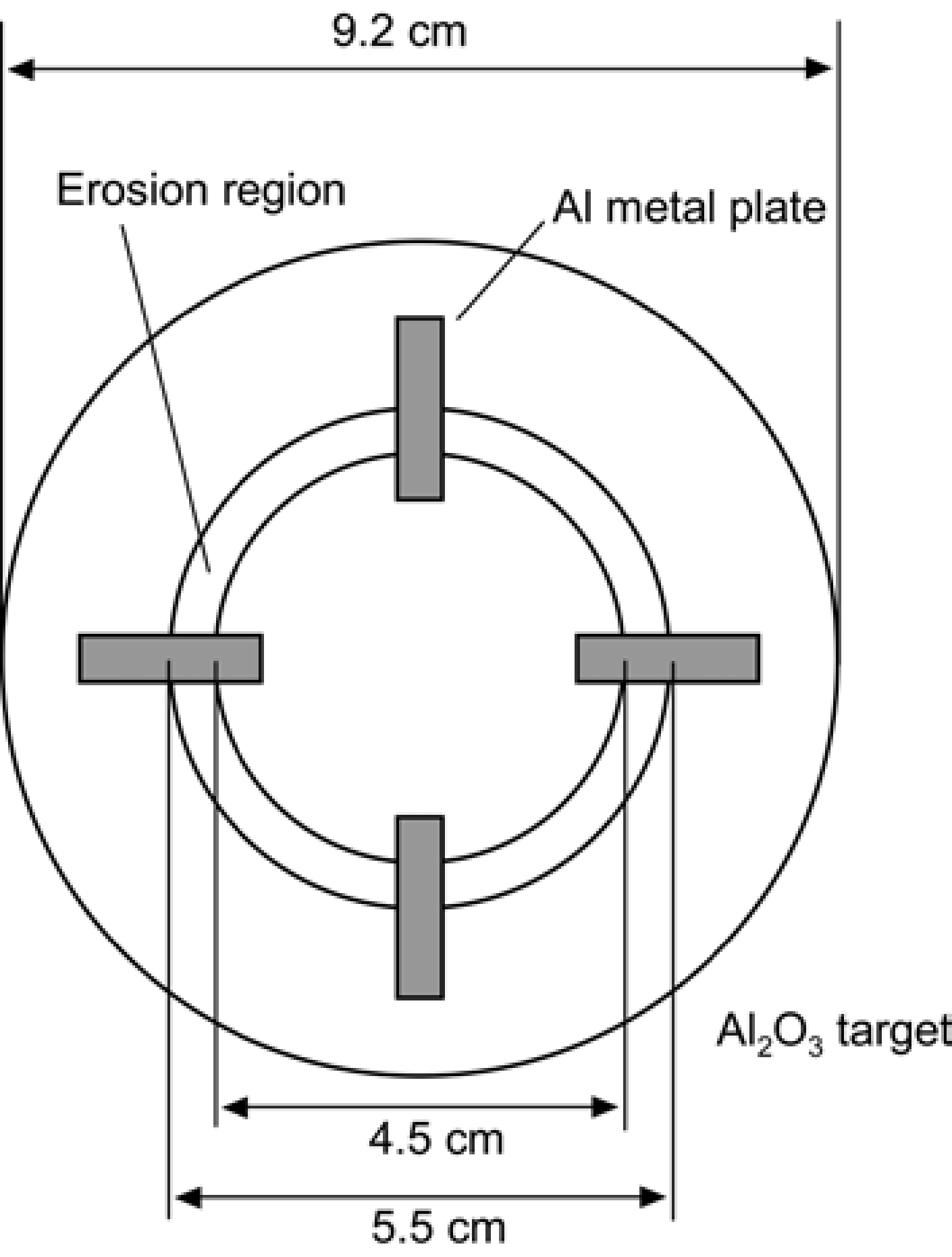
Fig. 8. Data retention characteristics for the sample with Al content of 50 %.

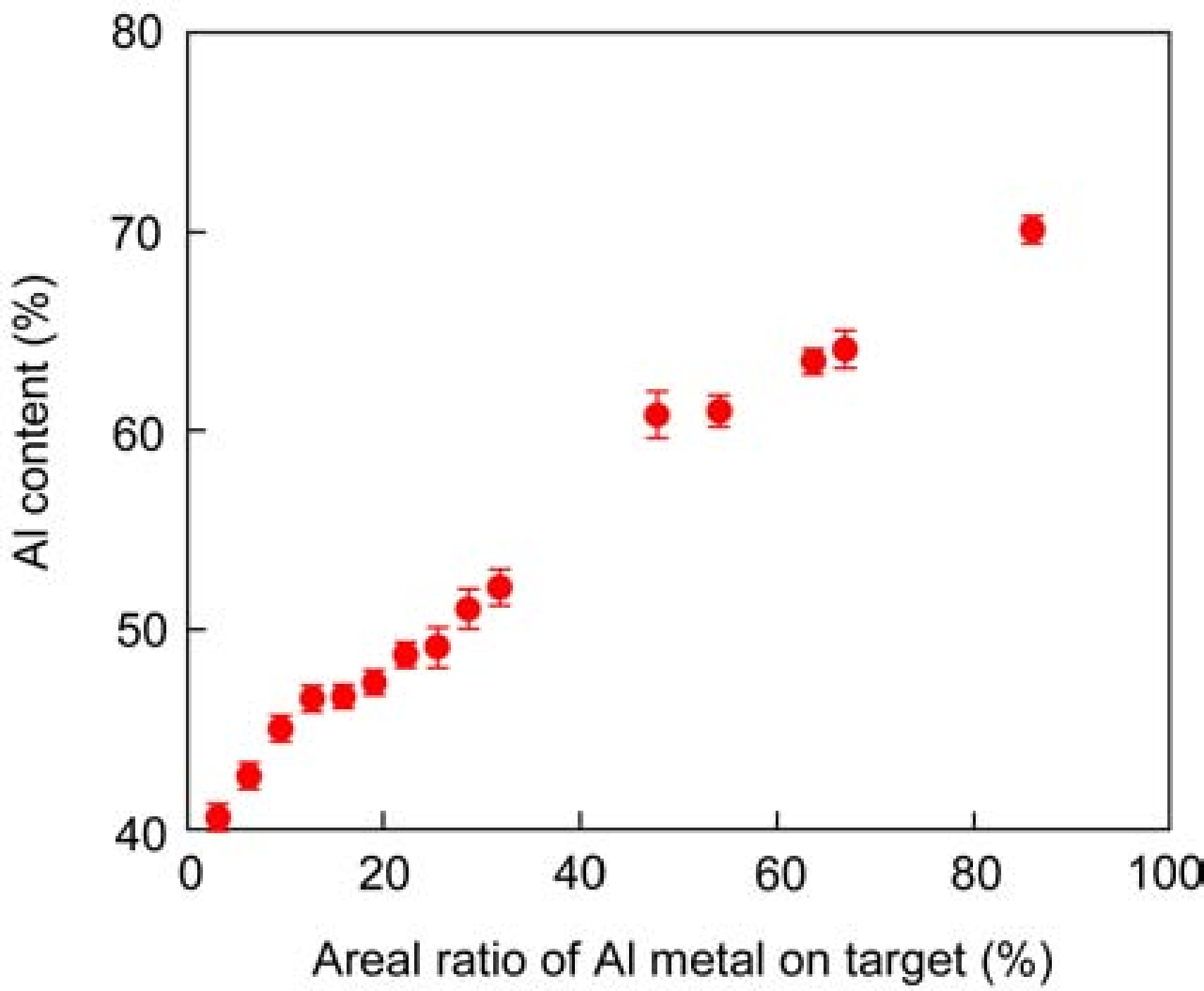
Fig. 9. Data retention characteristics for the sample with Al content of 58 %.

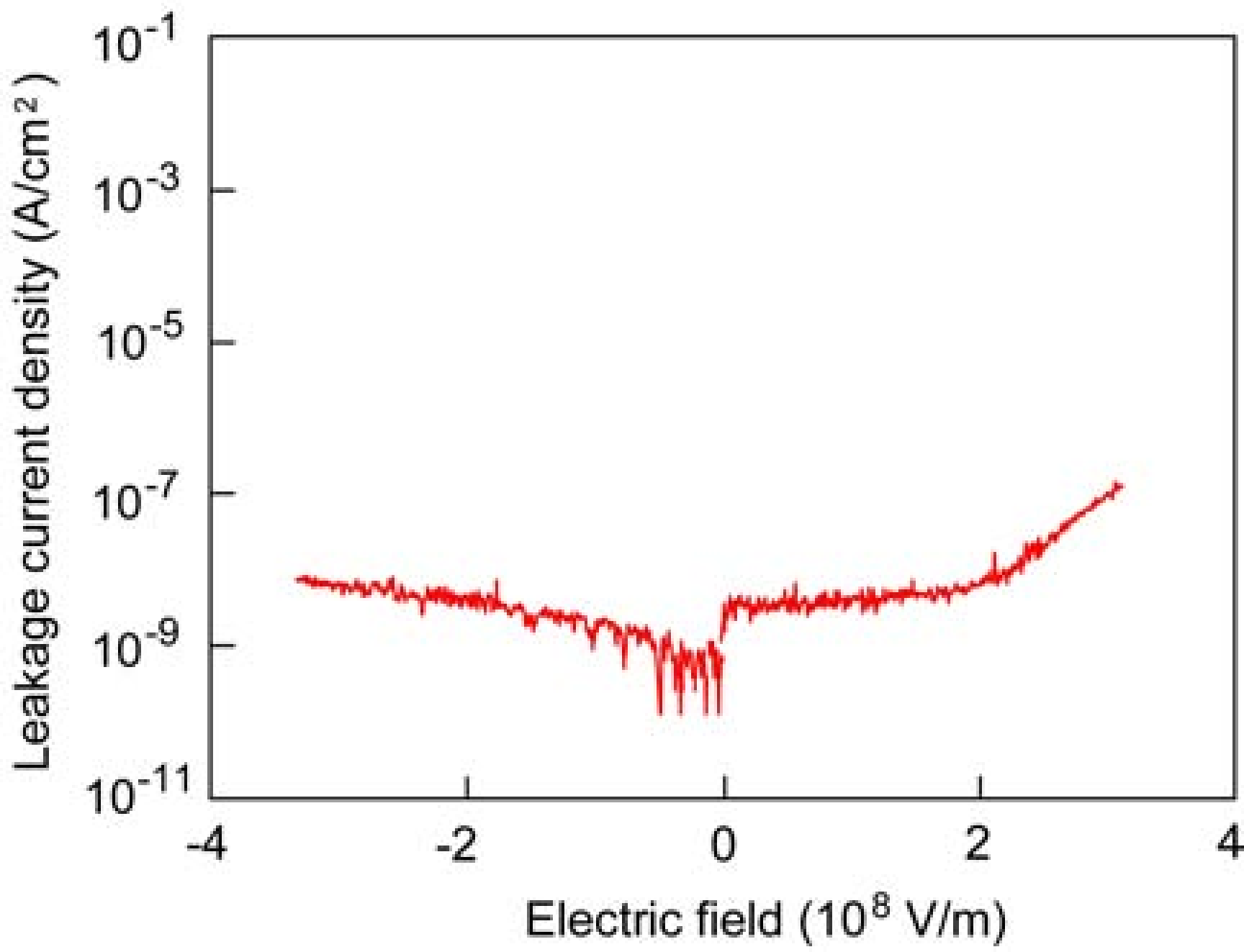

Gate
Al
7.3 nm
Al_2O_3
RF sputter
5.4 nm
Al-rich Al_2O_3
RF co-sputter
2.0 nm
SiO_2
Thermal oxidation
n-Si

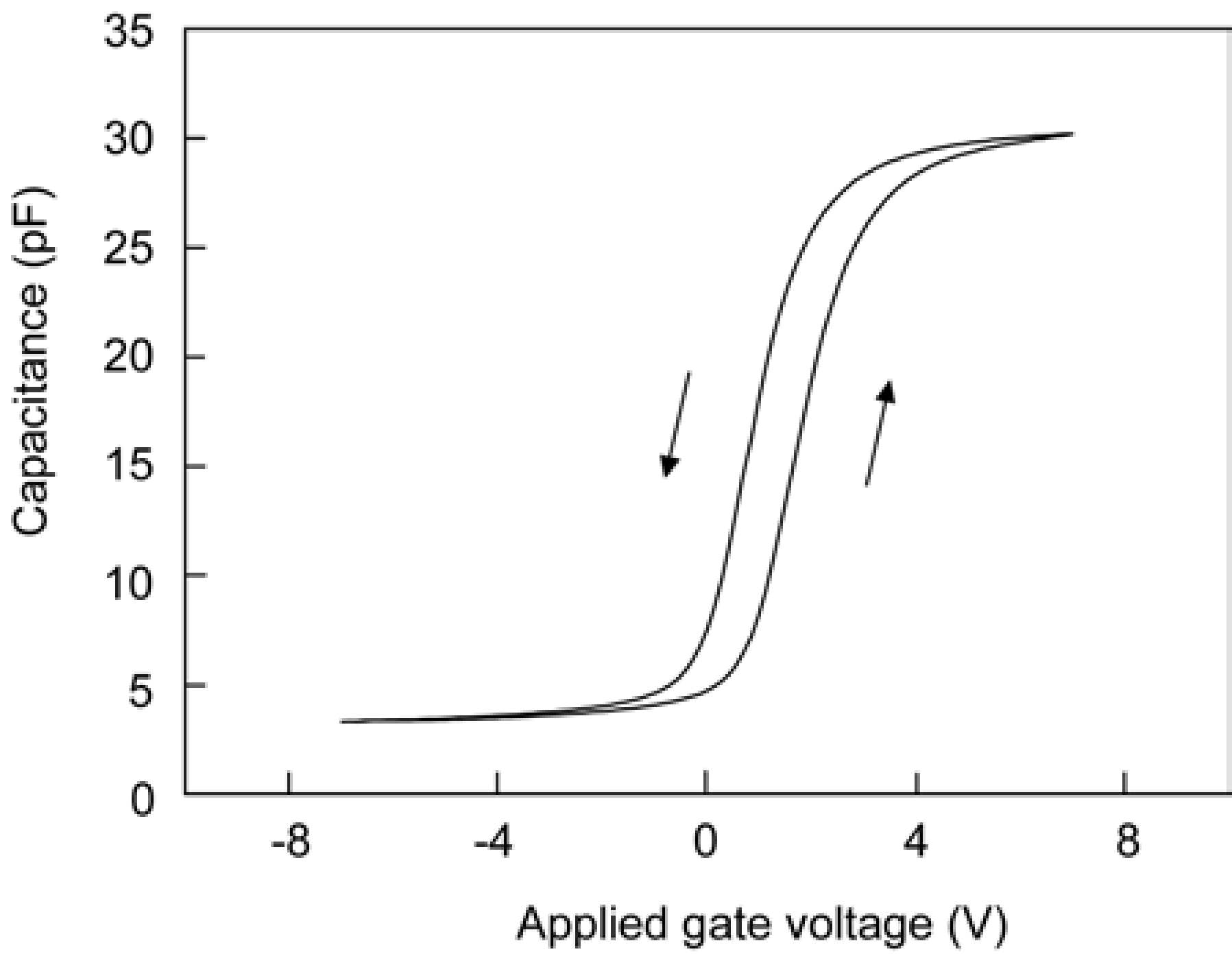

2.0 nm
5.4 nm
7.3 nm
n-Si
SiO2
Al-rich Al2O3
Al2O3
Al
0.7 eV
2.8 eV
2.4 eV
1.1 eV
Al:50%
Fermi level
Localization level

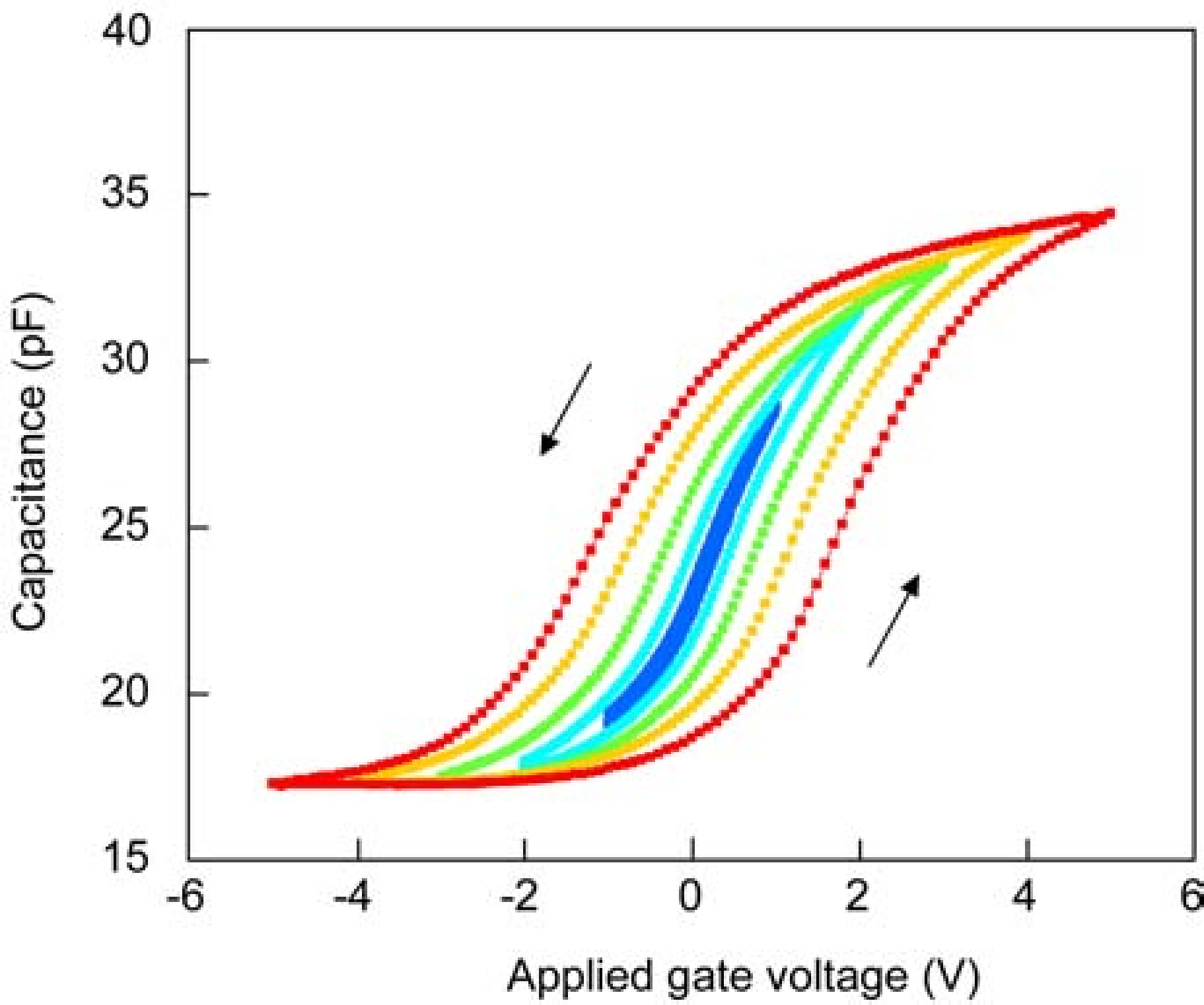

Wafer
MFC
Ar
Al metal plate
Al_2O_3 target
(9.2 cm ϕ)
S
N
S
Vacuum
Blocking capacitor
~
RF generator
(13.56 MHz)

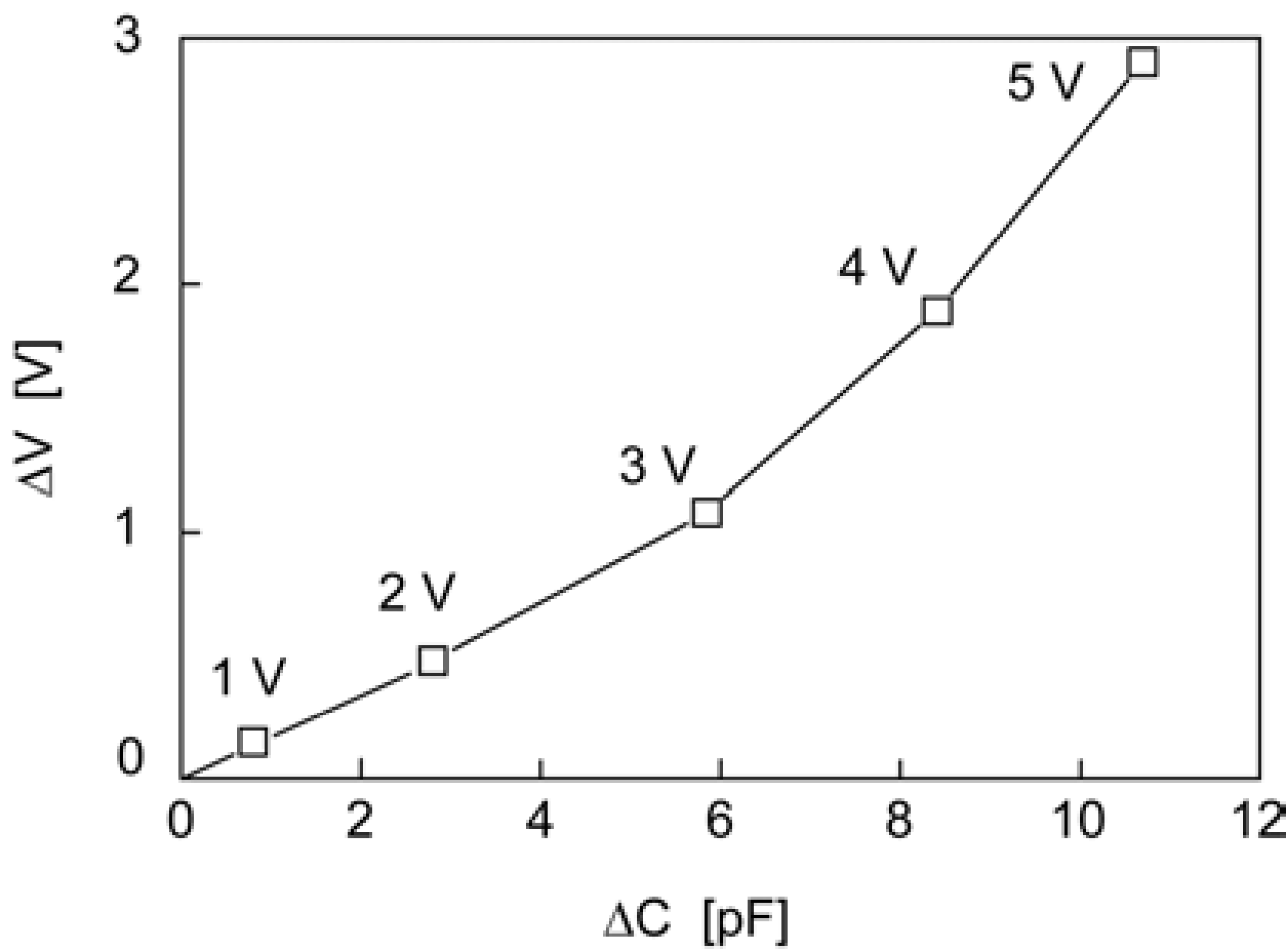

9.2 cm
Erosion region
Al metal plate
Al_2O_3 target
4.5 cm
5.5 cm

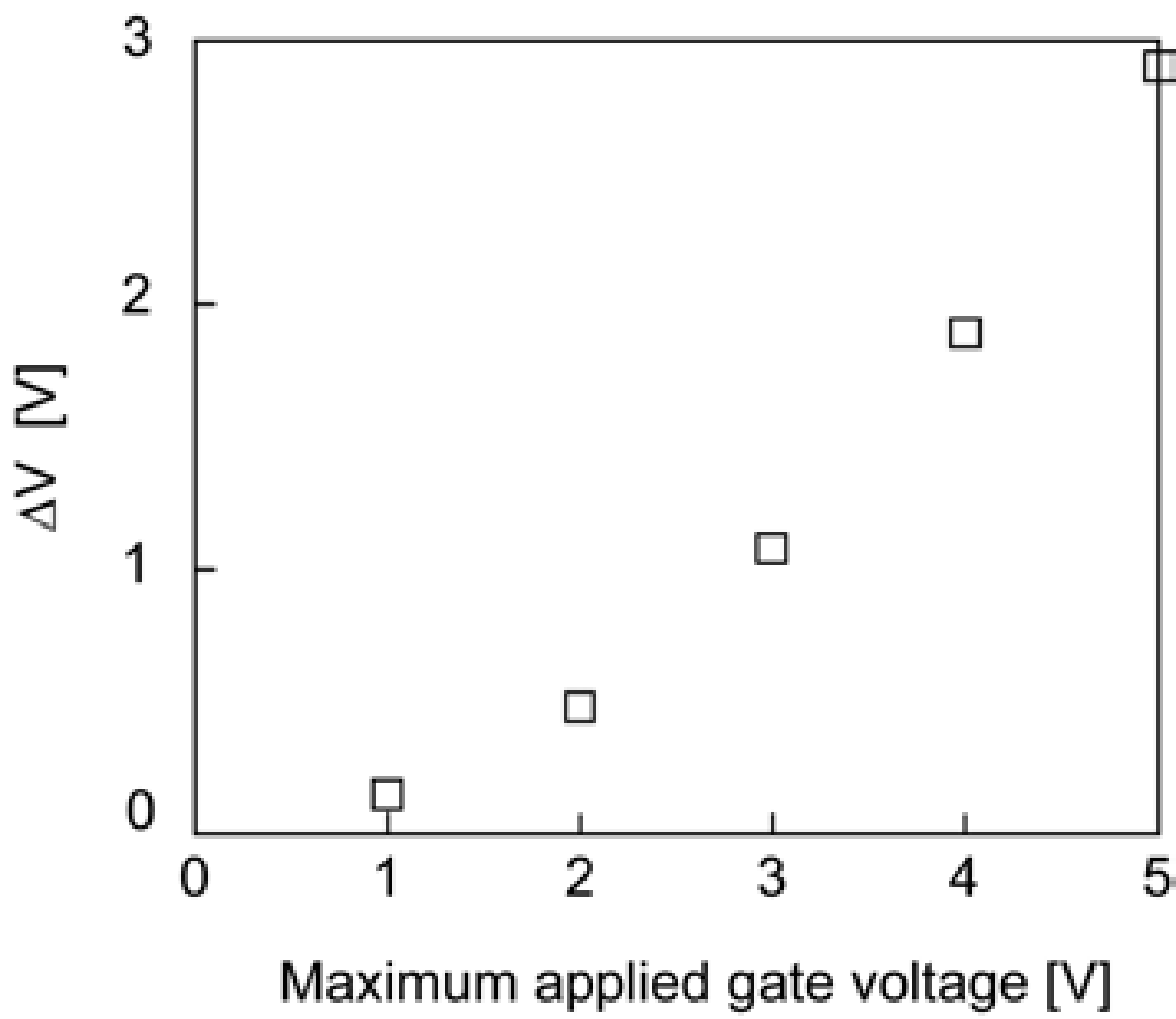

80
70
60
50
40
Al content (%)
0
20
40
60
80
100
Areal ratio of Al metal on target (%)

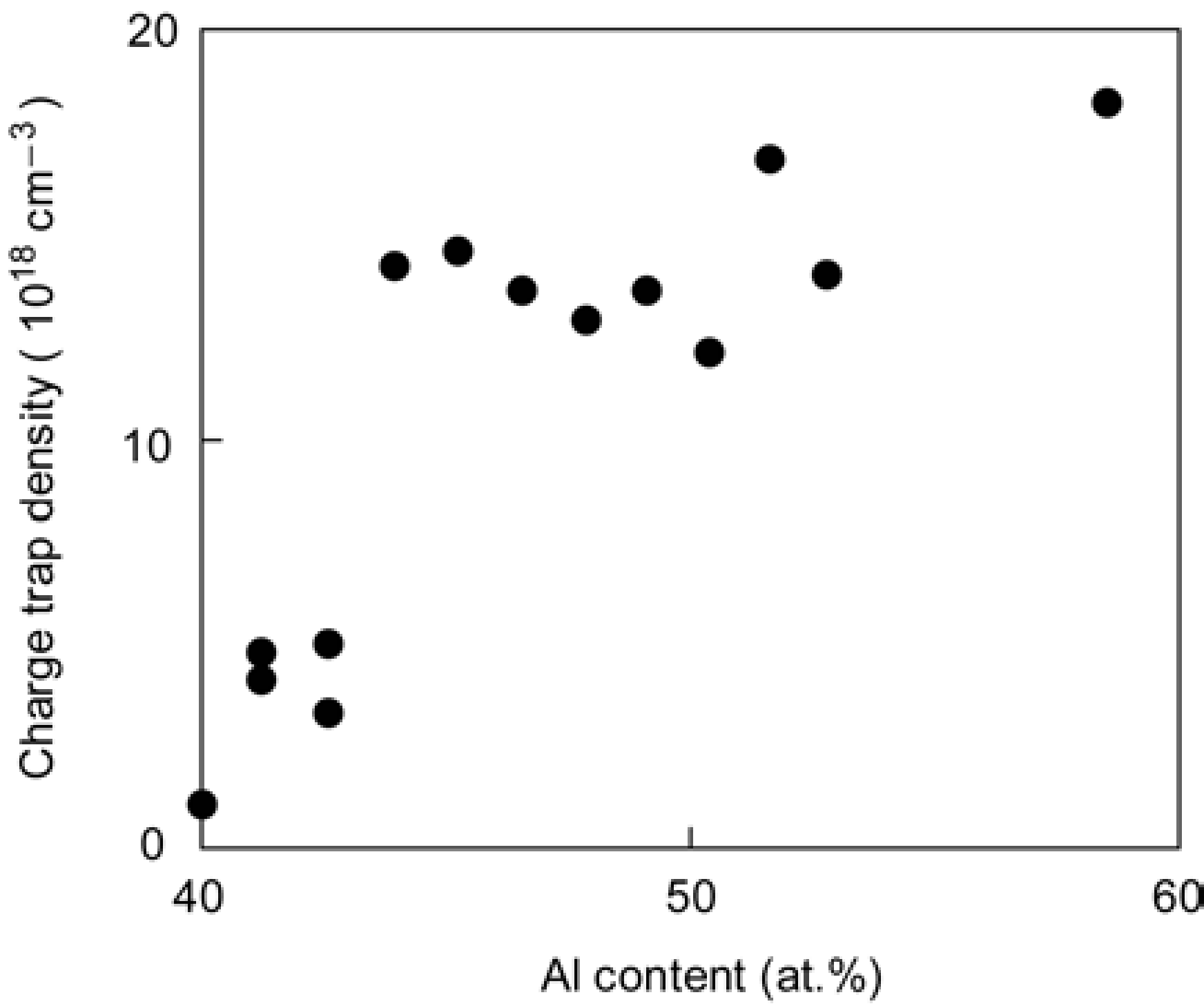

Leakage current density (A/cm²)
10⁻¹
10⁻³
10⁻⁵
10⁻⁷
10⁻⁹
10⁻¹¹
-4
-2
0
2
4
Electric field (10⁸ V/m)

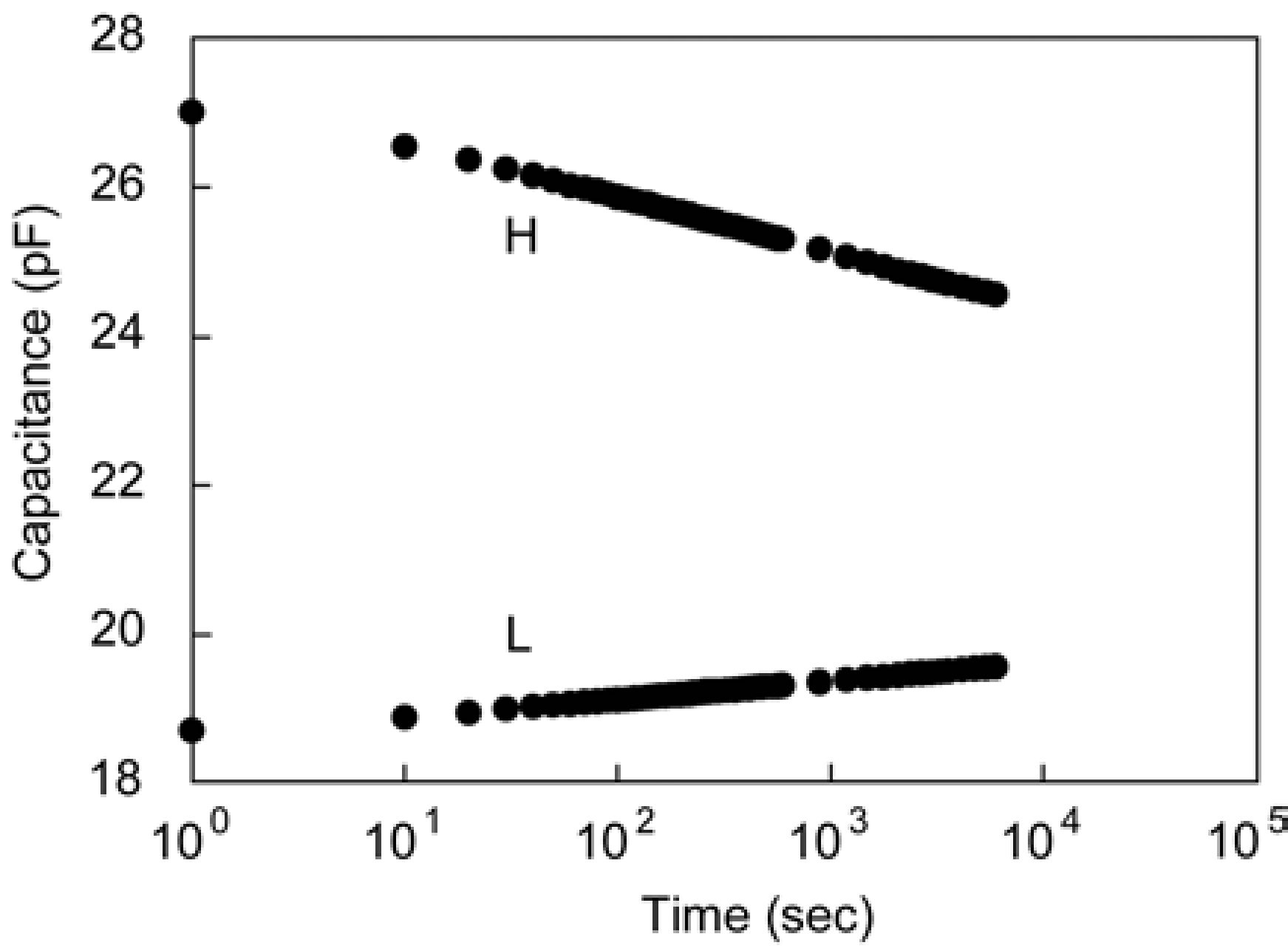

35
30
25
20
15
10
5
0
Capacitance (pF)
-8
-4
0
4
8
Applied gate voltage (V)

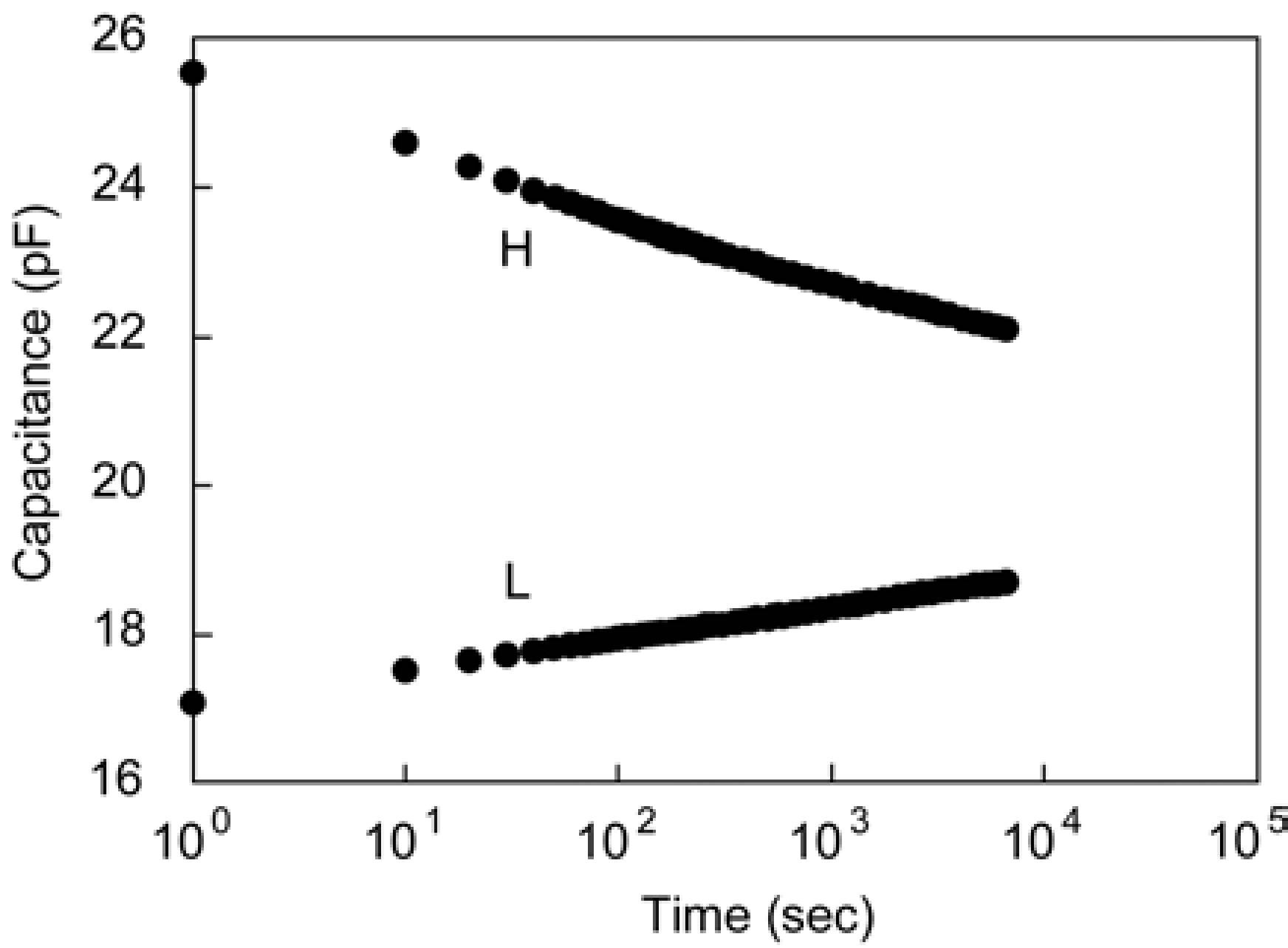

40
35
30
25
20
15
Capacitance (pF)
-6
-4
-2
0
2
4
6
Applied gate voltage (V)


3
2
1
0
ΔV [V]
0
2
4
6
8
10
12
ΔC [pF]
1 V
2 V
3 V
4 V
5 V


3
2
1
0
ΔV [V]
0
1
2
3
4
5
Maximum applied gate voltage [V]


20
10
0
Charge trap density (10^{18} cm^{-3})
40
50
60
Al content (at.%)


28
26
24
22
20
18
Capacitance (pF)
H
L
10^0
10^1
10^2
10^3
10^4
10^5
Time (sec)


26
24
22
20
18
16
Capacitance (pF)
H
L
10^0
10^1
10^2
10^3
10^4
10^5
Time (sec)

Q1, Q2 No problem

L20 Silicon

L216 $C_{Al_2O_3}$ are

L222 $C_{Al_2O_3}$

L254 metal–nitride–oxide–

L265 10–nm square

L267 silicon–oxide–

L268 nitride–oxide–silicon

L299 10–nm square

L348 second edition,