# GaAs- MISFETs with insulating gate films formed by direct oxidation and by oxinitridation of recessed GaAs surfaces

# GaAs-MISFETs With Insulating Gate Films Formed by Direct Oxidation and by Oxinitridation of Recessed GaAs Surfaces

Masahide Takebe, Kazuki Nakamura, Narayan Chandra Paul, Koichi Iiyama, *Member, IEEE*, and Saburo Takamiya

***Abstract*—Direct oxidation by an ultraviolet (UV) and ozone process and oxinitridation (plasma nitridation after oxidation) of GaAs surfaces were used to form nanometer-scale gate insulating layers for depletion-type recessed gate GaAs-MISFETs. The drain current–drain voltage characteristics of the oxide gate devices exhibit lower transconductance (max. 40 mS/mm), lower breakdown voltage and smaller gate capacitance than the oxinitrided gate devices. The presence of hysteresis in the oxide gate devices is also apparent. The maximum transconductance of the oxinitrided gate devices is 110 mS/mm and they have a sharper pinch-off, compared to the oxide gate devices. In addition, no hysteresis is observed in their current voltage curves. The current gain cutoff frequency of 1.4 $\mu$m gate-length FETs for both types is 6 GHz. These results correspond well with results obtained from characterization of these insulating films.**

***Index Terms*—Field-effect transistors (FET), GaAs, metal–insulator–semiconductor (MIS), nitridation, oxidation.**

## I. Introduction

IT IS WELL known that for the gate structure of a field-effect transistor (FET), a metal–oxide–semiconductor (MOS) or metal-insulator-semiconductor (MIS) is essentially superior to a Schottky barrier. The availability of enhancement-type devices, the fact that they can be operated using a single source of power, the possibility of high temperature operation and the attribute of scalability, etc. are all features which maintain this superiority. However, due to complex and unsolved surface/interface related problems, compound semiconductor MIS gate devices have not yet been realized commercially. Deposition of insulator materials and the conversion of semiconductor surfaces into insulating layers have been studied by many researchers in order to realize a reliable MIS gate compound semiconductor device with good performance. As for the deposition method, $Ga_2O_3$ [1], $Ga_2O_3(Gd_2O_3)$ [2], wet chemical $SiO_2$ [3], $Si_3N_4$ after the formation of a Si interface control layer [4], etc. have been reported. These form 10–40-nm-thick insulating layers and good electrical performance has been reported. In this paper, we have studied the conversion method, because this method utilizes the inherent properties of the mother material, and therefore gives rise to the possibility of realizing an essentially reproducible process, once an appropriate combination of semiconductor materials, gases and process conditions have been found that gives an insulator with a good insulator/semiconductor (I/S) interface and good performance. However, the flexibility in material choice and the applicable process techniques of this method are very limited.

We have reported that an ultraviolet radiation and ozone (UV and ozone) process forms a nanometer scale GaAs oxide layer that can suppress leakage current [5]. The thickness of this layer is proportional to square root of the process period. We also reported that GaAs-MOSFETs and InAlAs/InGaAs-MOSHEMTs with such oxide layers could be operated even beyond their flatband voltage [6]–[8], although dips in transconductance and the hysteresis were apparent in their current–voltage (*I–V*) curves. In order to overcome these problems, we studied the effect of nitridation upon bare and oxidized GaAs wafers from the points of view of the crystallographic structure near the interface and the electrical and photoluminescence performance. Hara *et al.* reported improved capacitance–voltage (*C–V*) characteristics of an oxidized GaAs-MIS diode by subjecting it to a helicon-wave-excited $N_2$ plasma treatment [9], although Trivedi *et al.* reported on $N_2$ plasma damage of an AlGaAs–InGaAs–GaAs system [10]. Our experimental results demonstrate that $N_2$ plasma nitridation after the UV and ozone oxidation forms a good quality GaAs-insulator interface with very little crystallographic disorder and improves both the electrical and the photoluminescence performance [11]–[13]. In order to check whether the beneficial effect of the $N_2$ plasma nitridation is reproduced in a device fabrication process, we simultaneously fabricated GaAs-MOSFETs (oxidation by UV and ozone only) and GaAs-MISFETs ($N_2$ plasma after the UV and ozone oxidation) and compared their performance.

Firstly, in this paper, the effects of nitridation upon oxidized (100) GaAs surfaces are briefly reviewed, then the structure, fabrication process, ant the dc and RF characteristics of GaAs-MISFETs are described and compared with GaAs-MOSFETs.

## II. Effects of Nitrogen Plasma

Nitrogen plasma severely damages the surface properties when it is applied to a bare GaAs surface, but it improves the interface properties when applied to an oxidized GaAs surface (becoming an nitrided oxide surface). The details of this are described in our previous papers [11]–[13].

Fig. 1 shows a cross-sectional transelectron microscope (TEM) image at the interface of oxinitrided GaAs, observed

Manuscript received Sept. 17, 2003; revised December 15, 2003. This work was supported under a grant from the Ministry of Public Management, Home Affairs, Posts and Telecommunication. The review of this paper was arranged by Editor C.-P. Lee.

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Digital Object Identifier 10.1109/TED.2003.823049

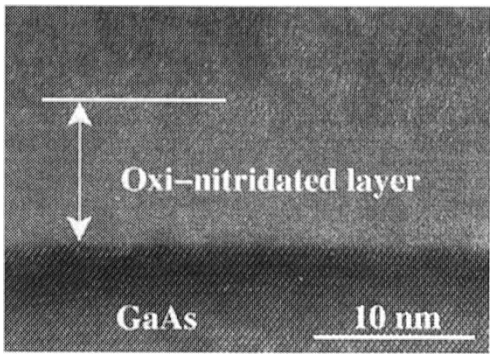


Fig. 1. TEM image of an oxinitrided GaAs/(100)n-GaAs structure observed from the $\langle 110 \rangle$ direction.

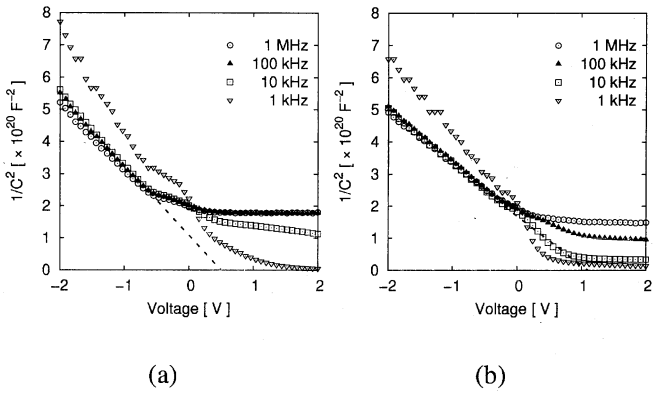


Fig. 2. (a) Measured $1/C^2$–$V$ characteristics of MIS diodes with insulating layers formed by oxidation for 8 h and (b) nitridation for 4 h after 8 h oxidation .

from $\langle 110 \rangle$ direction. This was formed by nitridation for 8 h in a $N_2$ plasma (RF power 250 W, $N_2$ flow rate 10 sccm) after oxidation for 8 h by an UV and ozone process at room temperature. The insulating layer thickness is about 8 nm. Very little crystallographic disorder and good interface flatness are observed. These characteristics are very effective in preventing the development of disorder related interface states and reducing electron scattering at the interface. The flatness is mainly realized by the long oxidation time rather than by the effect of nitridation. The oxidized GaAs layer is composed of Ga-oxide (mainly $Ga_2O_3$) which contains an amount of As-oxide (mainly $As_2O_3$). The nitridation process drives out the As and incorporates N in the GaAs-oxide layer changing it into a GaON layer with GaN especially near the interface. Moreover, the crystallographic order of the GaAs surface improves suggesting a decrease in the density of defects near the I/S interface. This accords well with the increased photoluminescence intensity of the oxinitrided surface compared to a simply oxidized surface. In nitridation of an oxidized GaAs layer, the $N_2$ plasma energy probably has an effect similar to annealing on the GaAs layer beneath the interface. The reverse leakage current of a MIS diode decreases with nitridation. Nitridation also improves the $C$-$V$ characteristics of the diodes in two respects. As these are directly related to a description of the dc and RF performance of the GaAs-MISFETs, they are shown in Fig. 2.

The $1/C^2$–$V$ relationship is generally used to find the barrier height of a Schottky junction rather than a MIS junction.

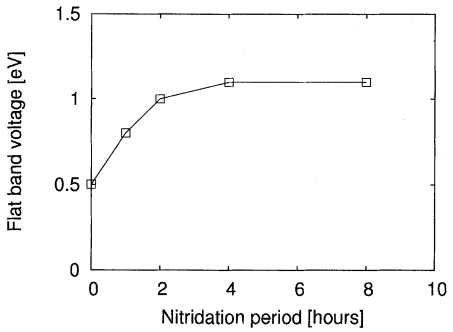


Fig. 3. Nitridation period dependence of flatband voltage obtained from $1/C^2$–$V$ characteristics.

However, as the insulator of our sample is very thin and negligibly small, compared to the depletion layer in reverse bias, the relationship holds even for a MIS diode and can be applied to obtain the flatband voltage. This is found by extrapolating the linear portion of the $1/C^2$–$V$ curve and finding the point at which this intercepts the voltage axis. The curve of a simply oxidized sample has two bends, one at around $-0.5$ V and the other at around $+0.2$ V. On the basis of the first bend the barrier height or flatband voltage of the oxidized sample is low (0.5 V). After 4 h of nitridation, the first bend completely disappears and the flatband voltage increases to $+1.1$ V, which is similar to previously reported values (0.8–1.1 eV) of Ni/n-GaAs Schottky barrier heights, suggesting a decrease in the positive I/S interface charge by nitridation. The dependence of flatband voltage on the nitridation time is shown in Fig. 3. This suggests that the oxidized samples initially have positive charge ($5 \times 10^{18}$ cm$^{-3}$ in the oxide or $2.8 \times 10^{12}$ cm$^{-3}$ at the interface [13]) which is neutralized by nitridation. The second bend, after nitridation, becomes sharper and shows a somewhat increased capacitance even at higher frequencies. This reflects the improvement of the I/S interface as explained by Passlack *et al.* [1]. The increase of the capacitance at high frequencies looks insufficient. However, as Xie *et al.* have demonstrated theoretically [14], even if the high frequency capacitance is increased sufficiently, this may be due to a parasitic effect of an area ($\sim$1 mm, in our MIS diode samples) between a broad Ohmic contact and the MIS junction (0.32 mm diameter).

## III. Structure and Fabrication

GaAs-MISFETs were fabricated on n-/S.I GaAs (100) wafers, of which the epitaxial layer thickness was 0.4 $\mu$m and the donor density was $3.0 \times 10^{17}$ cm$^{-3}$. After ultrasonic cleaning with acetone, the native oxide layer was removed by etching in buffered hydrofluoric acid. The epitaxial layer was etched down to 0.3 $\mu$m in order that the step height of the mesas in the later stages of the process would be reduced. The samples were then rinsed in de-ionized water. Drain and the source electrodes were formed by evaporating AuGe and Ni, followed by sintering at 360 °C for 2 min in $N_2$. After etching the mesas in a GaAs etchant ($H_3PO_4$:$H_2O$:$H_2O_2$ = 4:90:1), the wafer was coated with photo-resist which was patterned to define the gate areas. These areas were thinned to 0.18 $\mu$m. The etchant used to etch this recess was the same as that used for the mesa etch. Oxidation of the sample was done by an

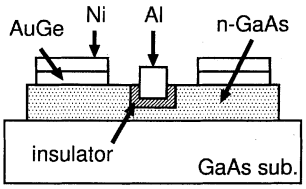


Fig. 4. Cross-sectional structure of the a GaAs-MISFET.

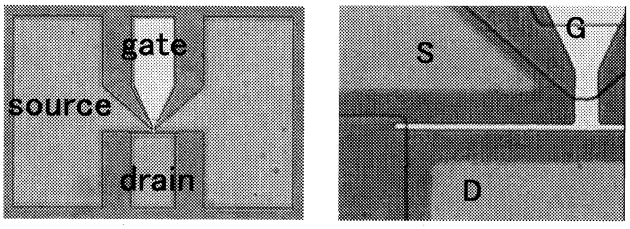


Fig. 5. Surface image of the fabricated GaAs-MISFET. (a) The whole area and (b) the gate portion.

UV and ozone process at 100 °C (SAMCO: UV and Ozone Cleaner UV-1) and the nitridation was done in an $N_2$ plasma at room temperature (SANYU: SHR-708). The plasma system was conditioned such that the RF power was 50 W and the $N_2$ flow rate was 10 sccm. Consequently, the oxinitrided layer was formed only in the recessed region. The oxidation period was fixed at 4 h and various nitridation periods of 0 h (hereafter denoted as the 4-0h sample), 1 h (4-1h sample) and 2 h (4-2h sample) were carried out depending on the wafers. Al was deposited and the unwanted parts removed by lift-off to leave only the gate electrodes. The cross-sectional structure of a fabricated GaAs-MISFET is shown in Fig. 4 and photographs of the surface are shown in Fig. 5. The gate width is 80 $\mu$m (40 $\mu$m $\times$ 2) and the gate length is 1 $\mu$m (designed).

In the above process, the photoresist for the gate pattern was used to define the area for four successive process steps; these were the recess etch, the oxidation, the nitridation and the gate electrode. This minimizes the possibility of contamination, automatically restricts the influence of the oxinitridation to within the recessed portion and self-aligns the electrode to the insulator as shown in Fig. 4. Both of the UV and ozone process and the $N_2$ plasma process ashes and thins the photo-resist. This, on the one hand implies that these are clean processes, but on the other restricts the operating conditions of the oxidation and nitridation systems so that the resist remains usable for the lift-off process. The RF power (50 W) of the treatment is much lower than that (250 W) used in our previous experiment [13].

## IV. DC Characteristics

The MIS diode characteristics between the gate and the source of GaAs MISFETs with different nitridation periods are shown in Fig. 6. The thickness of the insulating layer was estimated to be 6–8 nm from the oxidation time dependence of the oxide thickness [5], and it is not significantly altered by nitridation. The leakage current in the low reverse bias region is decreased depending on the nitridation time. The leakage

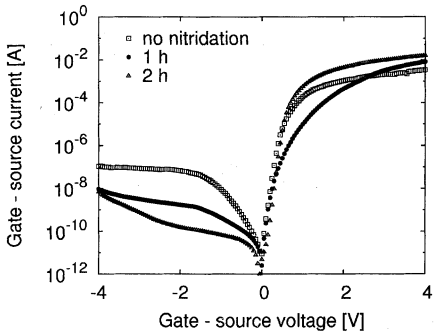


Fig. 6. Measured $I$–$V$ characteristics between the gate and source of GaAs-MISFETs.

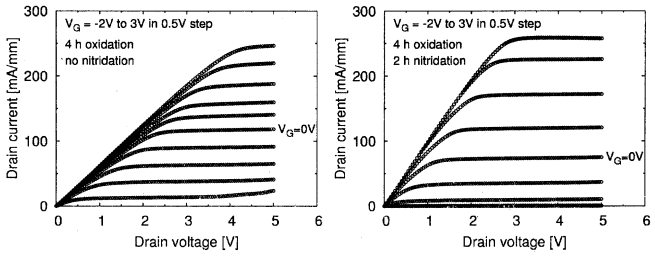


Fig. 7. Normalized dc characteristics of 1 $\mu$m GaAs-MISFETs for the (a) 4-0h and (b) 4-2h samples.

currents of nitrided samples were suppressed by up to three orders of magnitude compared to ones with simple oxide gates. The higher gradient of the reverse leakage current of the 4-2h sample in the high negative voltage region suggests generation of an inversion layer due to an improved barrier effect against holes. On the other hand, the small change in the low forward voltage region suggests that the barrier height of GaON against conduction band electrons is not so high. In the high forward voltage region, the 1h-nitridation sample exhibits a smaller current than the 2h-nitridation sample. This may be due to poorer Ohmic contact.

Fig. 7 shows the drain current versus drain voltage ($I_D$–$V_D$) characteristics of the 1-$\mu$m gate length (a) 4-0h and (b) 4-2h samples measured using a semiconductor parameter analyzer (Hewlett Packard: HP 4156A). The gate bias was changed from $-2$ to $+3$ V in 0.5 V steps. In the (a) 4-0h sample , the pinchoff is not good and a slight decrease in the transconductance is observed around the flatband voltage, similar to the GaAs MOSFETs, which we reported in 2002 [8], implying the existence of interface states. However, in the (b) 4-2h sample, the pinchoff is improved and a higher transconductance is realized. This indicates that the interface states are significantly reduced by 2 h of nitridation. Moreover, the drain-source resistance and the saturation voltage are decreased, suggesting that the gate voltage dependence of the depletion layer is increased partly due to recovery of the damaged layer.

Fig. 8 shows $I_D$–$V_D$ characteristics of 1-$\mu$m gate length GaAs-MISFETs (different samples from those shown in Fig. 7) during the drain voltage swing-up and swing-down processes. The simply oxidized sample has large hysteresis loops. In the negative gate bias region, the change in the gate voltage by

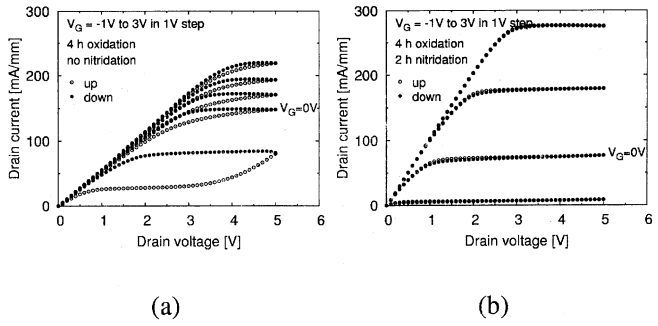


Fig. 8. Hysteresis curves of 1-$\mu$m GaAs-MISFETs for the (a) 4-0h and (b) 4-2h samples.

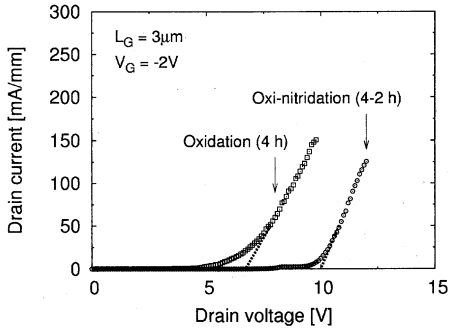


Fig. 9. Measured breakdown drain voltages of 3-$\mu$m gate length GaAs-MISFET at $V_G = -2$ V.

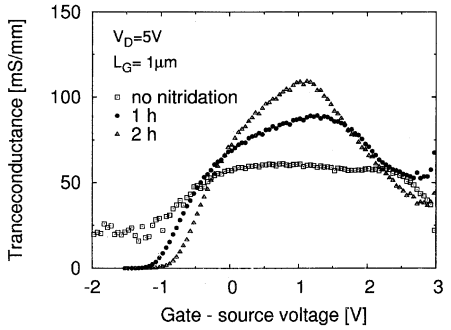


Fig. 10. Measured transconductances of 1-$\mu$m gate length GaAs-MISFETs at $V_D = 5$ V with different nitridation times after 4 h oxidation.

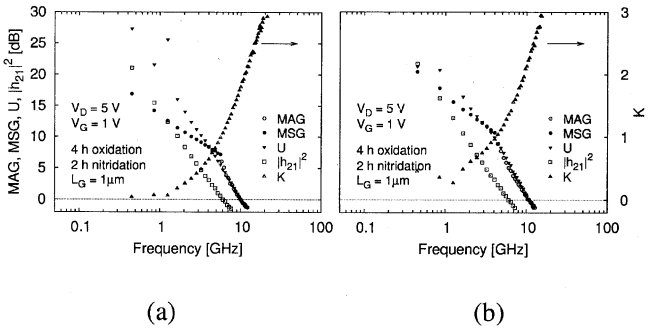


Fig. 11. RF characteristics of 1-$\mu$m GaAs-MISFETs for the (a) 4-0h and (b) 4-2h samples.

hysteresis is comparable to the flatband voltage improvement of 0.6 V by nitridation (Fig. 3). This results in an inaccurate transconductance when it is taken from the dc curves such as those in Fig. 7(a). On the other hand, the nitrided sample shows no hysteresis loops. This also implies that the former has a high density of traps and/or mobile ions near the interface or in the oxide layer, and that these are drastically reduced by nitridation.

Fig. 9 shows the measured drain breakdown voltages of 3-$\mu$m gate length GaAs-MISFETs at a gate bias of $-2$ V. The breakdown voltage of the 4-0h sample is about 6 V and that of the 4-2h sample is 10 V. This improvement may also be due to the reduced crystallographic disorder brought about by nitridation.

The gate voltage dependence of the transconductance of the 1 $\mu$m GaAs-MISFETs with different nitridation times, at a drain voltage $V_D$ of 5 V are shown in Fig. 10. It is quite obvious that the peak value of the transconductance increases with nitridation and that the pinch-off voltage is clear. One h of nitridation is insufficient and 2 h is not quite sufficient to minimize the interface problem. This agrees well with the previous experiment (Fig. 3) in spite of the different radio frequency (RF) powers. The simply oxidized sample has a maximum transconductance of 60 mS/mm, however this is not an accurate measurement due to the above mentioned hysteresis, and the data suggests that the actual transconductance is about 40 mS/mm with the base line shifted up by about 20 mS/mm due to hysteresis. The sample nitrided for 2 h has a peak transconductance of 110 mS/mm at a gate voltage $V_G$ of 1.1 V, which coincides with the flatband voltage obtained in Fig. 3. This coincidence is very important, because it implies that the device has no extra charge, neither in the insulator nor at the interface. On this point, the 4-2h sample has an ideal I/S interface.

## V. RF Characteristics

$S$ parameters of the samples from 500 MHz to 40 GHz were measured with a network analyzer (Hewlett Packard: 8722D). The frequency dependence of the maximum available gain (MAG), the maximum stable gain (MSG), the unilateral gain (U), the square of the absolute value of $h_{21}$ and the stability factor K, all obtained from the $S$ parameters, are shown in Fig. 11. The bias voltages are $V_D = +5$ V, $V_G = +1$ V. The current gain cutoff frequency $f_T$ and the maximum oscillation frequency $f_{\rm MAX}$ are estimated to be $f_T = 6$ GHz, $f_{\rm MAX} = 10$ GHz for both samples. The gate voltage dependence of $f_T$ and the transconductance of the 1-$\mu$m gate length (measured value 1.4 $\mu$m) GaAs-MISFET 4-2h sample are shown in Fig. 12. The maximum $f_T$ is observed at the peak transconductance.

The 4-0h and the 4-2h samples showed nearly equal RF performance despite the increase in the transconductance after nitridation. This suggests that nitridation causes an increase in the capacitance, because the current gain cutoff frequency is given by the transconductance divided by $2\pi$ and the gate-to-source capacitance. The capacitances calculated from measured $S_{11}$ parameters at 10 GHz with the bias condition of $V_D = +5$ V are shown in Fig. 13. The 4-2h sample has 2–3 times larger capacitance than the 4-0h sample. This is in contrast to the results shown in Fig. 2, where the capacitance of the nitrided MIS diode is nearly equal to that of the simply oxidized MIS diode in the high-frequency region (1 MHz). However, this contradiction is

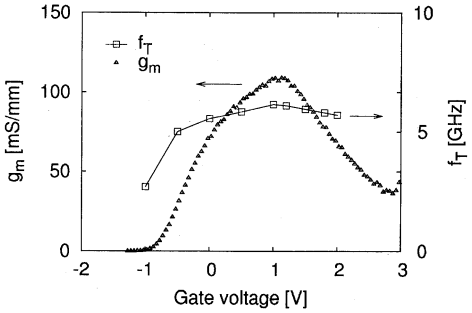


Fig. 12. Gate voltage dependence of $f_T$ and $g_m$ of the 1-$\mu$m gate length GaAs MISFET for the 4-2h sample.

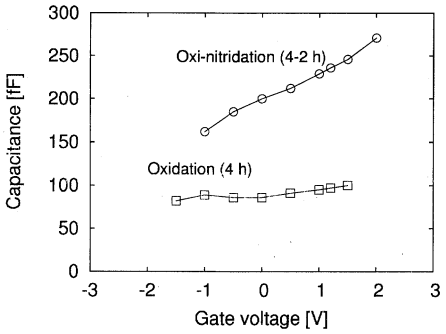


Fig. 13. Gate voltage dependence of the capacitances of 1-$\mu$m gate length GaAs-MISFETs from the $S_{11}$ parameters.

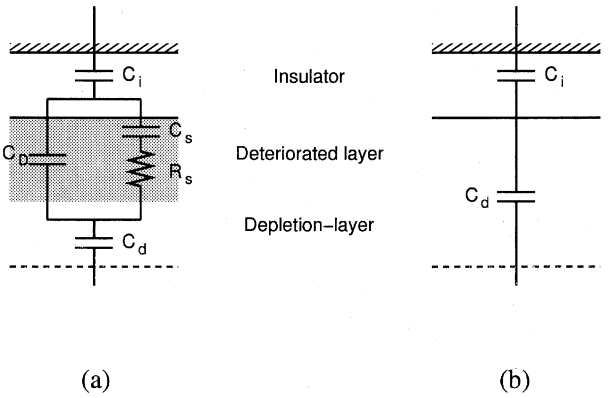


Fig. 14. (a) Equivalent MIS capacitance with an oxidized interface and (b) an oxinitrided interface.

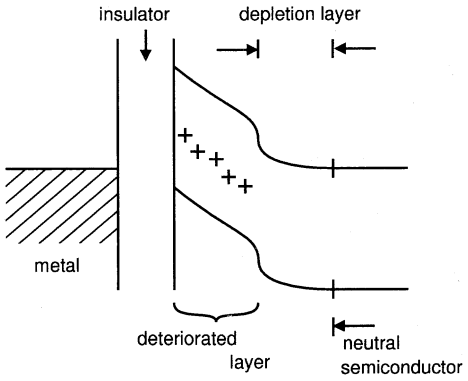


Fig. 15. Energy band diagram across the MIS portion of the simply oxidized sample.

explained by the theory developed by Xie *et al.* [14]; the parasitic effect of the area between the MIS junction and the Ohmic contact of the MISFET is very small compared to that of the MIS diode ($\simeq$1 mm), and thus the increase in capacitance by nitridation is observed directly in the FET. Nitridation increases both the transconductance and the capacitance, but the $f_T$ remains unchanged. As shown in Fig. 14(a), the total capacitance of the gate MIS junction of the 4-0h sample consists of the insulator capacitance $C_i$, the depletion layer capacitance $C_d$, the deteriorated layer capacitance $C_D$ and the interface state capacitance $C_s$, where the resistance $R_s$, in combination with $C_s$, determines the time constant of the charge/discharge process of the interface states.

Fig. 15 shows an energy band diagram across the MIS portion of the 4-0h sample. The deteriorated layer may be like an O doped semi-insulating semiconductor and contains positive charges as suggested by the first bend in the $1/C^2$–$V$ curves [13]. The increase in drain current in the positive gate voltage region far beyond the flatband voltage [Fig. 7(a)] suggests the existence of a high potential energy layer beneath the gate insulator only, outside of which the whole n-layer is normal. Obviously, the latter limits the maximum available drain current. Remarkably, although not perfectly, nitridation converts the deteriorated layer into a normal layer and increases $C_D$, but decreases $C_s$ and $R_s$ as shown in Fig. 14(b). This is the main reason for the increased capacitance as well as the increase in the transconductance. An additional reason may be the increase in the dielectric constant of the insulator. Nitridation increases $C_i$ by changing the GaAs-oxide into GaON, a similar effect to that of changing $SiO_2$ ($\varepsilon_r = 3.8$) to $Si_3N_4$ ($\varepsilon_r = 7.8$) in silicon technology. Since $C_s$ does not respond at microwave frequencies, only the changes of $C_D$ and $C_i$ are observed in $S_{11}$. Thus, the capacitance at 10 GHz, especially in the forward bias region, is increased by nitridation, reflecting the increase of $C_D$ and $C_i$.

## VI. Conclusion

We have demonstrated GaAs-MISFETs with an oxinitrided gate insulating layer formed by a combination of UV and ozone oxidation process and a $N_2$ plasma nitridation process in order to solve the problems associated with GaAs-MOSFETs reported in [8]. The oxinitrided gate device (GaAs-MISFET) exhibited smaller leakage current than the simple oxide gate device. Furthermore, it showed good pinch-off, no hysteresis, higher breakdown voltage and higher transconductance (110 mS/mm) with no dip at the flatband voltage, suggesting the existence of very little interface charge. This concurs with previous investigates of the structural and electrical properties of the oxinitrided n-GaAs layers. However, the GaAs-MISFET and GaAs-MOSFET showed a nearly equal current gain cutoff frequency of 6 GHz and a maximum oscillation frequency of 10 GHz. This is due to the increased capacitance.

In this experiment, in order to minimize thinning of the photoresist, an RF power of 50 W was used for exciting the $N_2$ plasma, which is much lower than that used in our previous experiment [13]. The authors have not yet found the optimum nitridation

period under such low power conditions. However, the coincidence between the gate voltage for the maximum transconductance (Fig. 10) and the flatband voltage suggests that a period of 2 h is not far from the optimum. When a plasma is applied to a wafer that is covered with a thin insulator, the insulator buffers the radical bombarding effect of the plasma and partly changes the effect into an annealing effect. The former causes deterioration of a semiconductor surface, but the latter possibly improves it. This deterioration/improvement ratio may depend on the insulator thickness and the plasma power; i.e., a lower power is preferable for the case of a thin insulator.

## ACKNOWLEDGMENT

The authors would like to thank Prof. N. Ohtsuka and K. Higashimine, JAIST for the TEM images.

## REFERENCES

[1] M. Passlack, M. Hong, E. F. Schubert, G. J. Zydzik, J. P. Mannaerts, W. S. Hobson, and T. D. Harris, "Advancing metal-oxide-semiconductor, theory: Steady-state nonequilibrium condtions," *J. Appl. Pys.*, vol. 81, no. 11, pp. 7647–7661, 1997.

[2] F. Ren, M. Hong, W. S. Hobson, J. M. Kuo, J. R. Lothian, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen, and A. Y. Cho, "Demonstration of enhancement-mode p- and n-channel GaAs MOSFETs with $Ga_2O_3(Gd_2O_3)$ as gate oxide," *Solid-State Electron.*, vol. 41, no. 11, pp. 1751–1753, 1997.

[3] M. P. Houng, Y. H. Wang, C. J. Houang, S. P. Huang, and J. H. Houng, "Quality optimization of liquid phase deposition $SiO_2$ films on gallium arsenide," *Solid-State Electron.*, vol. 44, pp. 1917–1923, 2000.

[4] Y. G. Xie, S. Kasai, H. Takahashi, C. Jiang, and H. Hasegawa, "A novel InGaAs/InAlAs insulated gate pseudomorphic HEMT with a silicon interface controllayer showing high, DC- and RF-performance," *IEEE Electron Device Lett.*, vol. 22, pp. 312–314, July 2001.

[5] T. Sugimura, T. Tsuzuku, T. Katsui, Y. Kasai, T. Inokuma, S. Hashimoto, K. Iiyama, and S. Takamiya, "A preliminary study of MIS diodes with nm-thin GaAs-oxide layers," *Solid-State Electron.*, vol. 43, pp. 1571–1576, 1999.

[6] Y. Kita, Y. Ohta, N. C. Paul, K. Iiyama, and S. Takamiya, "Depletion and accumulation mode operation of GaAs MISFETs with nm-thin gate insulating layers formed by UV & ozone," in *Proc. Int. Symp. Compound Semicond.*, Tokyo, Japan, 2001, p. 56.

[7] M. Nasuno, K. Nakamura, Y. Yamamura, K. Iiyama, and S. Takamiya, "Enhancement and accumulation mode operation of GaAs MISFETs and InAlAs/InGaAs MISHEMTs with nm-thin gate oxide layers," in *Proc. Int. Conf. on Solid-State Devices and Materials*, Nagoya, Japan, 2002, p. 506.

[8] K. Iiyama, Y. Kita, Y. Ohta, M. Nasuno, S. Takamiya, K. Higashimine, and N. Ohtsuka, "Fabrication of GaAs MISFET with nm-thin oxidized layer formed by UV & ozone process," *IEEE Trans. Electron Devices*, vol. 49, pp. 1856–1862, Nov. 2002.

[9] A. Hara, F. Kasahara, S. Wada, and H. Ikoma, "Effects of helicon-wave excited $N_2$ plasma treatment on fermi-level pinning," *J. Appl. Phys.*, vol. 85, no. 6, pp. 3234–3240, 1999.

[10] V. P. Trivedi, C. H. Hsu, B. Luo, X. Cao, J. R. Lorach, F. Ren, S. J. Pearton, C. R. Abernathy, E. Lambers, M. Hoppe, C. S. Wu, J. Sasserath, J. W. Lee, and K. Mackenzie, "The effect of $N_2$ plasuma damage on AlGaAs/InGaAs/GaAs high electron mobility transistorts. I. dc characteristics," *Solid-State Electron.*, vol. 44, pp. 2101–2108, 2000.

[11] N. C. Paul, Y. Ohta, D. Tezuka, M. Nasuno, Y. Yamamura, T. Inokuma, K. Iiyama, and S. Takamiya, "Quality improvement of oxidized-GaAs/n-GaAs structure by nitrogen plasma treatment," in *Proc. Indiurn Phosphide and Related Materials Conf.*, Stockholm, Sweden, 2002, p. 217.

[12] N. C. Paul, D. Tezuka, T. Inokuma, K. Iiyama, and S. Takamiya, "Effect of oxidation and/or nitridation of (100) n-GaAs surface," in *Proc. Workshop on Fundamentals and Applications of Advanced Semiconductor Devices*, 2002, p. 253.

[13] N. C. Paul, K. Nakamura, M. Takebe, A. Takemoto, T. Inokuma, K. Iiyama, S. Takamiya, K. Higashimine, N. Ohtsuka, and Y. Yonezawa, "Structural and electrical characterization of oxidated, nitridated and oxi-nitridated (100) GaAs surfaces," *Jpn. J. Appl. Phys.*, vol. 42, pp. 4264–4272, 2003.

[14] Y. G. Xie, K. Takahashi, H. Takahashi, J. Chao, S. Kasai, and H. Hasegawa, "Surface passivation of epitaxial multi-layer structures for InP-based high speed devices by an ultrathin silicon layer," in *IEICE Tech. Dig.*, vol. J84-C, 2001, p. 872.

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