Simultaneous enlargement of SRAM read/write noise margin by controlling virtual ground lines

doi: 10.1109/NEWCAS.2010.5603927

Simultaneous Enlargement of SRAM Read/Write Noise Margin by Controlling Virtual Ground Lines

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***Abstract*—The SRAM operating margin in 65nm technology is analyzed. The peak characteristic in the read margin versus the supply voltage was found to be caused by the channel length modulation effect. Controlling the memory cell virtual ground line proved to be effective in enlarging the operating margin simultaneously in the read and the write operations. A simple optimum circuit which does not require any dynamic voltage control is proposed, realizing an improvement in the operating margin comparable to conventional circuits requiring dynamic voltage control.**

I. INTRODUCTION

Advanced LSIs, such as System-on-a-Chips (SoCs) and microprocessors, continuously require more and more SRAM storage capacity to improve their performance. Recently, the progress of process technology has enabled over one hundred million bits of SRAM to be included in a chip [1]. Shrinking the physical dimensions of the SRAM, however, is becoming difficult because fluctuations of the device characteristics increase remarkably with the reduction of transistor area [2], [3]. Such fluctuation degrades memory cell stability both in the read and the write operations, so that any increase in bit capacity is limited.

To stabilize the SRAM memory cell, we have to consider both the read and the write operations, because their stabilizing conditions usually work in opposition. Several circuit techniques have been proposed to stabilize the SRAM memory cell. Controlling the word line voltage in the read operation increases the static noise margin (SNM) [4], [5], and the read noise margin. Weakening the power supply of the memory cell in the write operation increases the write noise margin (WNM) [4]-[7]. Although these circuit techniques are effective, they require complicated voltage control circuits which reduce the design simplicity and process portability.

In general, the SNM is supposed to increase as the supply voltage becomes higher. There are, however, some cases under certain circuit conditions in which the SNM does not improve, even if the supply voltage increases [4], [8]. This indicates the possibility of further optimization of the memory cell voltage to improve stability.

In this paper, we make a detailed analysis of the read and the write operations of the SRAM memory cell. Especially in the read operation, we clarify the reason, using a simple model, why the SNM does not increase steadily as the supply voltage increases. Then, we propose the optimum circuit and voltage condition to realize maximum memory cell stability.

II. ANALYSIS OF THE READ OPERATION

A. Definition of the read noise margin

Fig.1(a) shows a memory cell circuit in the read operation. The memory cell ground line (MCGL) is set to GND level, bit lines (BL_L and BL_R) are fixed to the power supply voltage (V_{DD}) and the word line voltage (V_{WL}) changes from 0V to V_{DD}. Then, the data stored in N1 and N2 are read out to the BL_L and BL_R, respectively. The static noise margin (SNM) is used to estimate the stability of the memory cell in the read operation [9]. Fig.1(b) shows a butterfly curve which consists of a pair of transfer curves of the storage nodes, N1 and N2, when the V_{WL} is fixed to V_{DD}. The SNM, as shown in Fig.1(b), is defined as one side length of the maximum inscribed square. If the sizes of the two maximum inscribed squares are different, the SNM is defined as the smaller one.

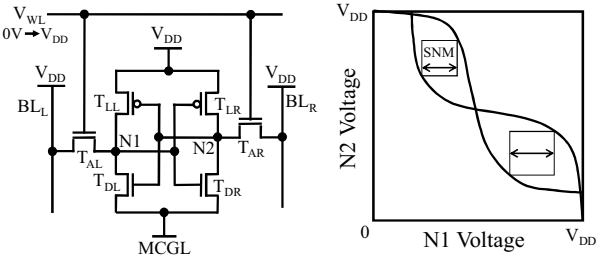

Fig.1. (a) SRAM read operation and (b) definition of SNM

B. Voltage dependence of SNM

We simulated the voltage dependences of the SNM in various cases using the 65nm SPICE parameter [10]. Transistor sizes are summarized in Table 1. Gate lengths of all transistors are 65nm. As shown in the table, β_t is the gate width ratio of the driver transistor to the access transistor. In the simulation, the V_{DD} is simultaneously applied to the word line and the bit lines. Fig.2 shows the dependence of the SNM on the V_{DD}. As the V_{DD} increases, the SNM initially increases, and then decreases in all three cases of β_t=1.0, 1.25, and 1.5. That is, the SNM peaks at a certain V_{DD}. This tendency becomes more obvious in smaller β_t. The peak position shifts to the higher voltage side as the β_t increases.

Although the saturating characteristic of the SNM versus V_{DD} has been suggested in previous works [4], [8], studies have given neither a detailed analysis nor a description of the peak characteristic. Ref. [8] indicates that the saturation is caused by the channel length modulation effect.

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Table 1. Transistor sizes

	Gate width [nm]	
T_{LL} , T_{LR}	80	
T_{AL} , T_{AR}	80	
T_{DL} , T_{DR}	β_t=1.0	80
	β_t=1.25	100
	β_t=1.5	120

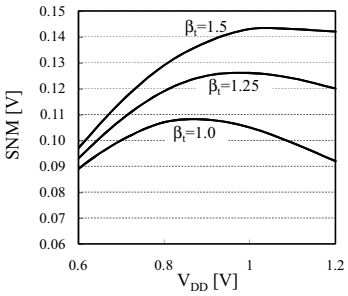


Fig.2. Dependence of SNM on V_{DD}

From the following analysis, we found that the peak characteristic is also caused by the same channel length modulation effect. As our aim is not to reproduce the simulation results precisely, but to clarify the origin of the peak, we started from the following simple equations of transistor I-V characteristics.

$$I_{p,linear} = \beta_p (V_{gs} - V_{thp} - \frac{V_{ds}}{2}) V_{ds} (1 + \lambda_p V_{ds}) \quad (1)$$

$$I_{p,sat} = \frac{\beta_p}{2} (V_{gs} - V_{thp})^2 (1 + \lambda_p V_{ds}) \quad (2)$$

$$I_{n,linear} = \beta_n (V_{gs} - V_{thn} - \frac{V_{ds}}{2}) V_{ds} (1 + \lambda_n V_{ds}) \quad (3)$$

$$I_{n,sat} = \frac{\beta_n}{2} (V_{gs} - V_{thn})^2 (1 + \lambda_n V_{ds}) \quad (4)$$

The suffixes p and n represent the pMOS and the nMOS transistors, respectively. $I_{n,linear}$ and $I_{p,linear}$ are the transistor currents in the linear region and $I_{n,sat}$ and $I_{p,sat}$ in the saturation region. β_p and β_n are transconductances, V_{thp} and V_{thn} are the threshold voltages, and λ_p and λ_n are the channel length modulation parameters. V_{ds} and V_{gs} denote the drain and the gate voltages to the source voltage, respectively.

We determined the parameters, β_p, β_n, λ_p, λ_n, V_{thp} and V_{thn} in (1)-(4), by fitting the memory cell butterfly curves to the SPICE simulation results in β_t=1.0. The determined values of the parameters are $-V_{thp}=V_{thn}=0.2$V, $-\lambda_p=\lambda_n=1$, $\beta_p=4.5\times10^{-5}$, $\beta_n=1.3\times10^{-4}$ for the driver transistors and $\beta_n=7.8\times10^{-5}$ for the access transistors

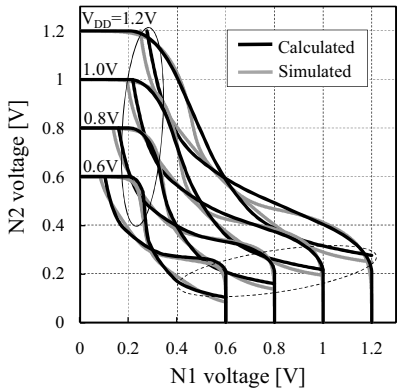


Fig.3. Butterfly curves at various V_{DD}

Fig.3 shows the butterfly curves at the supply voltages of 0.6V, 0.8V, 1.0V and 1.2V. The black lines are the numerically calculated results from equations (1)-(4) after the fitting. The gray lines are the results of the SPICE simulation. In spite of our rough approximation, the calculated lines closely correspond to the simulated results and possess the characteristics of real butterfly curves. Both curves obviously show the decrease of SNM in high V_{DD}.

To investigate the influence of the channel length modulation effect on the SNM, we measured the SNMs of the calculated butterfly curves by changing λ_p and λ_n. Fig.4 shows the dependence of the SNM on the V_{DD} for various λs, where $\lambda=-\lambda_p=\lambda_n$ and β_t=1.0. Although the SNM increases at a steady rate as the V_{DD} increases for λ=0, peak characteristics appear for λ=0.2-1.0. The V_{DD} peak decreases as the λ increases. This phenomenon is caused by the decrease of the SNM at high V_{DD}. This decrease becomes more noticeable as the λ increases. In Ref. [8], the peak does not appear clearly because the SNM is observed within a small range of λ.

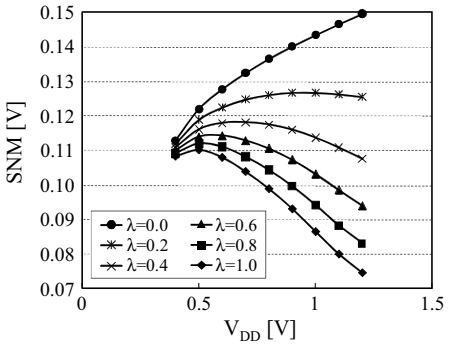


Fig.4. Dependence of SNM on V_{DD} for various λs

The reason for the SNM decrease at high V_{DD} is explained as follows.

(i) The current of the driver transistor in the saturation region increases by the channel length modulation effect as the V_{DD} increases. This causes the rapid decrease of the butterfly curve (see the solid ellipse in Fig. 3). As a result, the SNM is reduced.

(ii) As the current of the access transistor in the saturation region increases, the low level of the butterfly curve goes up as the V_{DD} increases (see the dotted ellipse in Fig. 3). This also reduces the SNM.

Generally, the SNM increases as the V_{DD} increases. On the other hand, when the channel length modulation effect increases, the SNM is reduced. Thus, the opposite effects induce the peak on the curve of SNM versus V_{DD}.

It should be noted that the higher peak of the SNM is obtained by raising the memory cell ground line, the MCGL in Fig.1, instead of lowering the V_{DD}. The SPICE simulation in Fig.5 shows the dependence of the SNM both on the MCGL voltage and the V_{DD}. The V_{DD} is set to 1.2V in controlling the MCGL and the MCGL is set to 0V in controlling the V_{DD}. In this simulation, the bodies (p-well) of the nMOS transistors are tied to the GND level. Raising the MCGL voltage is more effective in improving the SNM than decreasing the V_{DD}. As a result, the peak SNM in raising MCGL voltage is more than 15% larger than that in decreasing V_{DD} for all cases of β_t=1.0, 1.25 and 1.5. This is because raising the MCGL voltage causes an increase in the threshold voltage of the nMOS transistors in the memory cell by a reverse body bias effect. Increasing the threshold voltages of the nMOS transistors, especially those in the access transistors, improves the SNM.

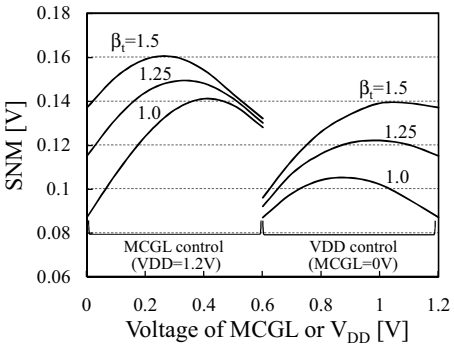


Fig.5. Dependence of SNM on MCGL and V_{DD}

C. *Consideration of Vth fluctuation*

In the deep-submicron process, random fluctuations of the device characteristics are noticeable [2], [3]. Therefore, we have to take such fluctuations into account when discussing the improvement of read stability. We investigated the dependence of read stability on transistor threshold voltages because their fluctuations strongly affect read stability. Fig.6 shows a simulated circuit which demonstrates the worst case for a read operation. The $\Delta V_{thn}(>0)$ and the $\Delta V_{thp}(<0)$ represent the random fluctuations of the threshold voltages of the nMOS and pMOS transistors (V_{thn} and V_{thp}), respectively. From the Stolk's equation [3] and the SPICE parameters [10], we estimated that the standard deviations of the V_{thn} and V_{thp} (σV_{thn} and σV_{thp}) are 35.1mV and 34.3mV. As an example of the worst case, the ΔV_{thn} and the ΔV_{thp} are set to $3*\sigma V_{thn}$ and $3*\sigma V_{thp}$. The simulation is carried out by examining whether the read operation is possible or not for various V_{thn} and V_{thp}. Here, we changed the VTH0s of nMOS and pMOS SPICE parameters [10] to vary the V_{thn} and the V_{thp}.

Fig.7 shows the simulation results. Five curves express the boundaries of the "PASS" region and the "FAIL" region for the MCGL of 0.0V, 0.1V, 0.2V, 0.3V and 0.4V at β_t=1.0. In the "PASS" region, the read operation is successful and in the "FAIL" region, the read operation fails. The "PASS" region gets larger as the MCGL increases to 0.3V. For example, although the read operation fails for an MCGL of less than 0.2V when V_{thn}=0.5V and V_{thp}=0.4V, it is successful for an MCGL voltage above 0.2V. For an MCGL higher than 0.4V, however, the "PASS" region shrinks. These behaviors closely match the results (Fig.5) in the earlier section. Therefore, the read margin can be improved by increasing MCGL voltage, even if there are random fluctuations in the threshold voltages.

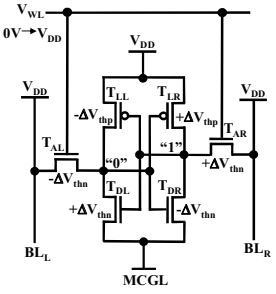


Fig.6. Simulated circuit

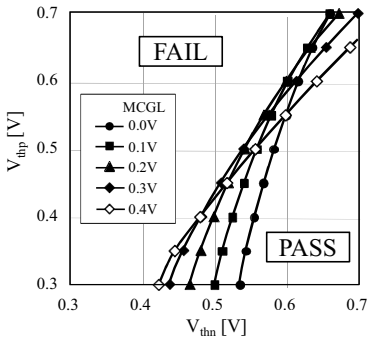


Fig.7. Boundary curves between "PASS" and "FAIL"

III. IMPROVEMENT OF THE WRITE MARGIN

A. *Definition of the write noise margin*

Fig.8(a) shows a memory cell circuit in the write operation. The memory cell power line (MCPL) and the MCGL are usually connected to the V_{DD} and GND, respectively. Initially, the storage nodes (N1 and N2) are "1" and "0", respectively, and the word line voltage (V_{WL}) is 0V. Then, the left and right bit lines (BL_L and BL_R) are set to GND and V_{DD}, respectively, and the V_{WL} rises from 0V to V_{DD}. Fig.8(b) shows the voltages of the storage nodes in the write operation. When the N1 and N2 voltages turn over together at a certain value of V_{WL} (V_W), the write operation is complete. We adopt the definition of write noise margin (WNM) as the voltage difference between V_W and V_{DD} [11]. A larger WNM corresponds to an easier write operation.

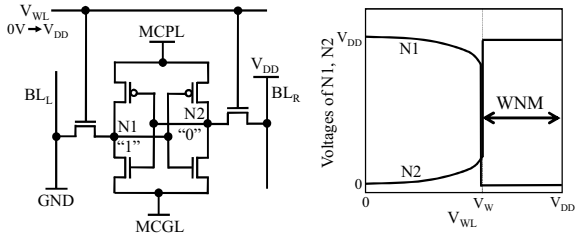


Fig.8. (a) SRAM write operation and (b) Definition of WNM

B. *Voltage dependence of the WNM*

The WNM can be increased by lowering the memory cell supply voltage [4]-[7]. There are two possible means to lower the memory cell supply voltage. One is decreasing the MCPL (CASE1) and the other is increasing the MCGL (CASE2).

We simulated the voltage dependences of the WNM in CASE1 and CASE2. Fig.9 shows the simulation results. The WNM improves similarly in both Case1 and Case2, with voltage changes in the MCPL and MCGL. Also, the dependence of the WNM on the β_t is small. This is because the source-to-drain currents of the load transistor and the access transistor, T_{LL} and T_{AL} in Fig.1(a), mainly determine the WNM. Those currents are almost the same in both cases for any β_t, because the gate-to-source voltages are almost the same. Therefore, the stability of the SRAM memory cell in the write operation improves by increasing the MCGL as much as by decreasing the MCPL.

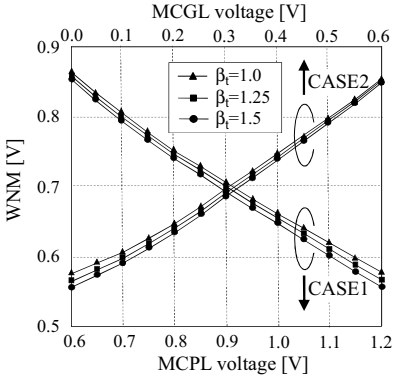


Fig.9. Dependence of WNM on V_{DD} and MCGL voltages

IV. OPTIMIZATION

A. Optimized circuit

The above analysis proves that controlling the MCGL is more effective in enlarging the operating margins simultaneously in the read and the write operations than in controlling the V_{DD} or the MCPL. Fig.10 shows the concept of the optimized SRAM circuit. The power supply of the memory cell is connected to the V_{DD} together with all the other circuits. Only the virtual ground line of the memory cell array, the MCGL, is separated from the ground lines of the other circuits and controlled by the "MCGL generator" circuit. The "MCGL generator" generates the optimum MCGL voltage to maximize memory cell stability. Unlike the case of MCGL=0V, under optimum MCGL, the stabilities of the memory cell both in the read and the write operations simultaneously improve. This circuit is quite simple when compared with conventional circuits [4]-[7] because there is no need to dynamically control the power line. The optimized MCGL voltage is constant and does not change during the read and write operations.

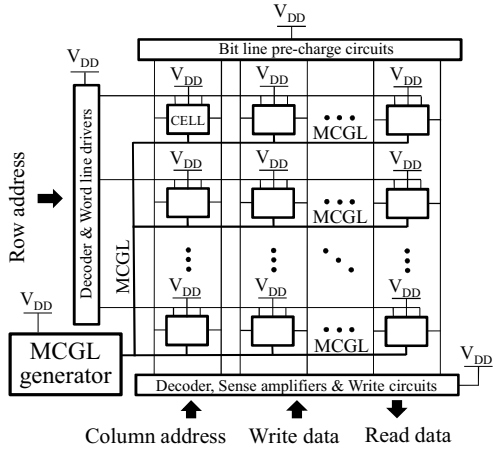
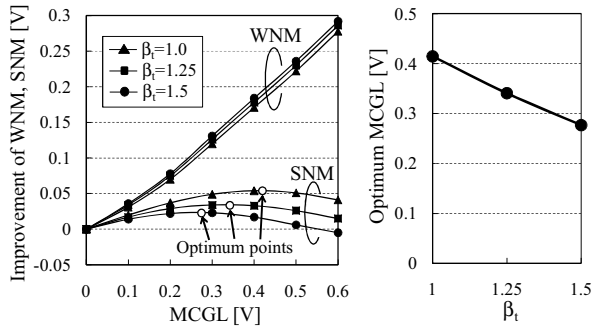


Fig.10. Concept of the optimized SRAM circuit



(a) (b)

Fig.11. (a) Improvement of WNM and SNM and (b) Optimum MCGL vs. β_t

B. Optimization of MCGL voltage

Optimum MCGL voltage can be determined from the above analysis. Fig.11(a) shows the dependence of WNM and SNM improvements on the MCGL voltage. These improvements are measured by subtracting the values of the WNM and SNM at MCGL=0V from those at each MCGL voltage. Improvement of the WNM increases steadily for the MCGL and is much higher than that of the SNM. Therefore, to create the optimum condition, we should select the maximum point of the SNM. Fig.11(b) plots the optimum MCGL voltage versus the β_t taken from Fig.10(a). For a β_t from 1.0 to 1.5, which is used in ordinary memory cell design, the optimum MCGL voltage varies from 0.41V to 0.28V. The improvement of the SNM at the optimum MCGL varies from 22mV to 53mV, which is comparable to that of the conventional read assist circuit [4]. We can maximize memory cell stability by using the optimum MCGL voltage.

V. CONCLUSION

From the analysis of the SRAM memory cell, both in the read and the write operations using 65nm SPICE, controlling the MCGL proved to be effective in simultaneously enlarging the SNM and the WNM. The channel length modulation effect created the peak characteristic in the SNM versus V_{DD}, which then enabled the SNM increase by raising the MCGL. We proposed the optimum SRAM circuit and MCGL voltage. The improvement of the SNM at the optimum MCGL voltage is comparable to that of the conventional read assist circuit. Because the channel length modulation effect will become greater and greater in the future, we are convinced that the proposed scheme will become more and more effective.

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