doi: 10.1109/MWSCAS.2011.6026367

Energy Dissipation Decrease During Adiabatic Charging of a Capacitor by Changing the Duty Ratio

Shunji Nakata[1], Hiroshi Makino[2], Shin'ichiro Mutoh[1], Masayuki Miyama[3], and Yoshio Matsuda[3]

[1]NTT Microsystem Integration Labs, Nippon Telegraph and Telephone Corp., Atsugi, Japan: nakata.shunji@lab.ntt.co.jp
[2]Faculty of Information Science and Technology, Osaka Institute of Technology, Osaka, Japan: makino@is.oit.ac.jp
[3]Graduate School of Natural Science, Kanazawa University, Kanazawa, Japan: matsuda@ec.t.kanazawa-u.ac.jp

***Abstract*— Adiabatic charging of a capacitor with a step down converter by changing the duty ratio is considered. First, for a profound understanding of the circuit, the general analytical solution of step down converter is considered. It is confirmed that the system can be resolved analytically and that the equilibrium state of current and voltage are consistent with SPICE simulation. Next, adiabatic charging by changing the duty ratio is investigated. From SPICE simulation, it is confirmed that energy dissipation is reduced to one-fourth when four-step charging is used. By increasing the step number, energy dissipation decreases to zero and dissipationless operation is achieved.**

I. INTRODUCTION

Recently, renewable energy is considered to be very important for achieving a sustainable society. In this area, energy storage is very important because the renewable energy from sources, such as wind power and solar power, is not continuously output. There are several ways to store the energy, such as lead-acid batteries, NiMH batteries, Li ion batteries, and supercapacitors. Among them, we believe that supercapacitors will become more important in future. Supercapacitors can be charged and discharged more than 100,000 times. Moreover, they can operate in the wide temperature region of -25 to 70 ^{o}C, which is wider than that of Li ion batteries. Further, supercapacitors exhibit significant higher volumetric power density. However, circuits for charging and discharging supercapacitors have not been well studied yet.

In this article, we demonstrate that adiabatic stepwise charging [1-5] is effective for reducing the energy dissipation when using a step down converter. We have already introduced an effective technique for both charging and discharging a capacitor in the same circuit [6]. As shown in Fig. 1, when charging, the circuit operates as a step down converter and current flows from X to Y. When discharging, it operates as a step up converter and current flows from Y to X. Charging and discharging are performed by changing the duty ratio stepwise. This means that the capacitor is charged stepwise during charging and energy is recovered (or discharged) stepwise to power supply E gradually.

However, in the circuit in Fig. 1, the reduction of energy dissipation has not yet been confirmed. In this article, we investigate this point in detail using SPICE simulation.

First, for a profound understanding of the circuit in Fig. 1, we analyze the general *LCR* circuit. The voltage and current values after the circuit reaches the equilibrium state are discussed analytically in Sec. II and discussed using SPICE simulation in Sec. III. Next, using the *LCR* circuit analysis, we perform the SPICE simulation of the adiabatic charging.

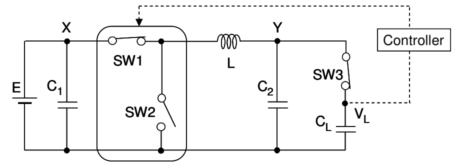

Fig. 1. A circuit that can charge and discharge a load capacitor adiabatically.

The energy dissipation is calculated when the capacitor is charged stepwise. It is clarified that, for four-step charging, energy dissipation decreases to one-fourth compared to the conventional constant voltage charging. This is described in Sec. IV.

II. LCR CIRCUIT ANALYSIS

For a more profound understanding of the circuit behavior in Fig. 1, we consider the general *LCR* circuit shown in Fig. 2(a). The $E_{ex}(t)$ is the external voltage. I is the current through the inductor and V is the voltage of capacitor. Here, we consider a periodic square wave as $E_{ex}(t)$. Using the duty ratio d, a period T, and a constant voltage E, we express $E_{ex}(t)$ in a period as

$$E_{ex}(t) = \begin{cases} E, & (0 \le t < dT) \\ 0, & (dT \le t < T) \end{cases}. \tag{1}$$

This $E_{ex}(t)$ is considered to be the same as the left part of the step down converter in Fig. 2(b). Therefore, analyzing a square wave means analyzing the step down circuit in Fig. 2(b). When $0 \le t < dT$ (mode 1) and $dT \le t < T$ (mode 2), the circuit equations are written as

$$L\frac{dI}{dt} + RI + V = E \text{ and } L\frac{dI}{dt} + RI + V = 0, \tag{2}$$

respectively. By connecting the solutions of (2), we can resolve these differential equations. The derivation will be discussed in detail elsewhere. Then, we have the expression of the current at the beginning of mode 1, I_n, as

$$I_n = c_1 e^{nk_1T} + c_2 e^{nk_2T} + c_3(n), \tag{3}$$

where n is the number of square waves from t=0, c_1 and c_2 are constant, and $c_3(n)$ is a function of n. k_1 and k_2 are characteristic solutions of (2) and are written as

$$k_1 = \frac{-R + \sqrt{R^2 - 4L/C}}{2L} \text{ or } k_2 = \frac{-R - \sqrt{R^2 - 4L/C}}{2L}. \tag{4}$$

The real part of k_1 and k_2 is always negative so that e^{nk_1T} and e^{nk_2T} become zero when n is large. Therefore, the converged value of I_n, I_f, is written as

$$\begin{aligned} I_f &= \lim_{n\to\infty} I_n = \lim_{n\to\infty} c_3(n) \\ &= \frac{CEk_1k_2}{k_2 - k_1}\left\{\frac{(e^{k_1(1-d)T} - e^{k_1T})}{1 - e^{k_1T}} - \frac{(e^{k_2(1-d)T} - e^{k_2T})}{1 - e^{k_2T}}\right\}. \end{aligned} \tag{5}$$

978-1-61284-857-0/11/$26.00 ©2011 IEEE

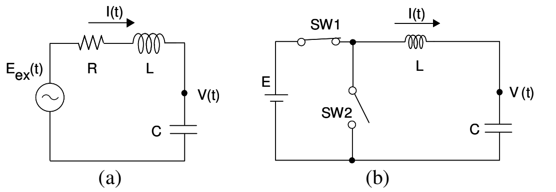

Fig. 2. (a) The general LCR circuit with external voltage $E_{ex}(t)$. (b) Step down converter. A switch is composed of nMOS and pMOS transistors.

In power electronics circuit, the switching frequency is sufficiently faster than the resonant frequency. Therefore, we have the relations k_1T<<1 and k_2T<<1. Then, using (5), we have

$$I_f = -\frac{d(1-d)TE}{2L}. \quad (6)$$

Regarding the converged current at the beginning of mode 2, I'_f, we can derive the relation $I'_f = -I_f$.

Regarding the voltage, we define V_n and V'_n as the voltage at the beginning of modes 1 and 2, respectively. Then, we define V_f and V'_f as $V_f = \lim_{n\to\infty} V_n$ and $V'_f = \lim_{n\to\infty} V'_n$. Then, using k_1T<<1 and k_2T<<1, we have

$$V_f = V'_f = dE. \quad (7)$$

Equation (7) is consistent with formula in power electronics. Regarding the current, the average current in the equilibrium state is zero so that the relation $I'_f = -I_f$ is reasonable.

III. SIMULATION OF EQUIRIBRIUM STATE

In this section, to verify (6), we investigate the I_f and I'_f of the circuit in Fig. 2(b) with SPICE. We used the 180-nm design rule. The transistor gate length L_g is 0.18 µm and gate widths of pMOS and nMOS W_p and W_n are 200 and 100 µm, respectively. E is 2 V. The gate voltage of SW1 and SW2 is changed from 0 to 3.3 V. Threshold voltages V_T's are 0.43 and −0.33 V in nMOS and pMOS, respectively. The body biases of nMOS and pMOS are GND and VDD, respectively.

The simulation result is shown in Fig. 3. L is 1, 10, or 20 µH. T, which corresponds to the switching period, is set to 0.1 µs. The duty ratio is changed as 0.2, 0.4, 0.6, and 0.8. It is clarified that the capacitance voltage $V(t)$ increases stepwise as 0.4, 0.8, 1.2, and 1.6 V, which are consistent with dE. Regarding the current, the current flows largely at the beginning of each step. After large flows of current, the circuit reaches the equilibrium state. This is common with L=1, 10, and 20 µH. The equilibrium current oscillates between two values. It is confirmed from Fig. 3 that the oscillation amplitude decreases when L increases. Fig. 4 is a magnification of Fig. 3 at t=154 µs. When L=1 µH, the current oscillates linearly between -23.9 and 23 mA. When L=10 and 20 µH, it oscillates between -2.4 and 2.4 mA and between -1.2 and 1.2 mA, respectively. With $d(1-d)TE/2L$, the theoretical values are 24, 2.4, and 1.2 mA, which are perfectly consistent with the SPICE simulation results. Therefore, the analytical formula is correct.

IV. SIMULATION OF ADIABATIC CHARGING

Here, we discuss the effectiveness of stepwise adiabatic charging. We set L to 800 µH in order to make the

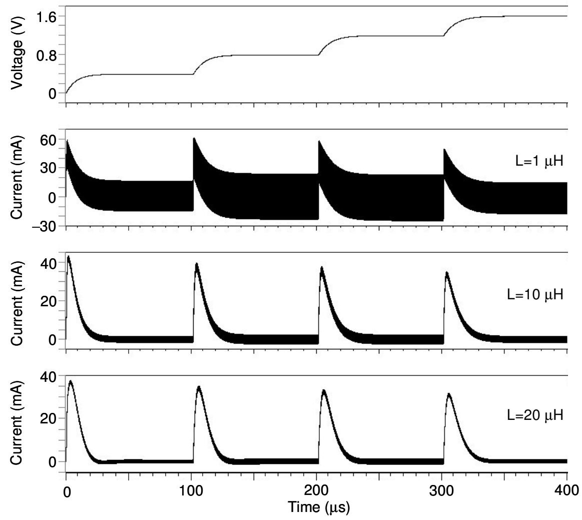

Fig. 3. V and I of step down converter when the duty ratio is changed stepwise.

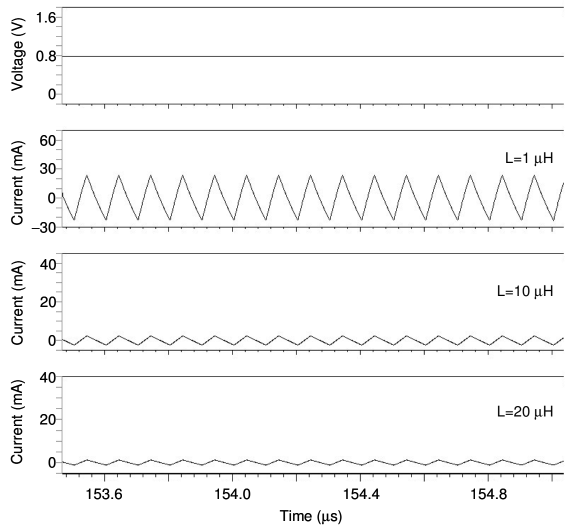

Fig. 4. Magnification of current in Fig. 3 at t=154 µs.

equilibrium current oscillation almost zero. By making I_f and I'_f zero, we can decrease the Joule heat at the equilibrium state. After setting L to 800 µH, we set C to 1, 20, 40, or 50 µF to investigate the adiabatic charging in detail. We discuss the change of the voltage and current in each case. In the following simulations, we set T to 1 µs.

Fig. 5 shows the simulation results for C=1 µF. The time period for each step charging is 1 ms. The average voltage almost changes stepwise. However, the voltage oscillates until it converges to the step value. Also, the current oscillates according to the $I=CdV/dt$. Due to the voltage oscillation, the voltage increases more than the expected step voltage. In particular, this voltage increase at the final step is not good for a device. We should decrease the voltage overshoot due to the oscillation. The oscillation occurs because k_1 and k_2 in (3) are complex. If k_1 and k_2 are real numbers, oscillation does not occur. To make k_1 and k_2 real numbers, the value of R^2-4L/C should be positive, so the C value should be increased.

Fig. 6 shows the simulation results for C=50 µF. The

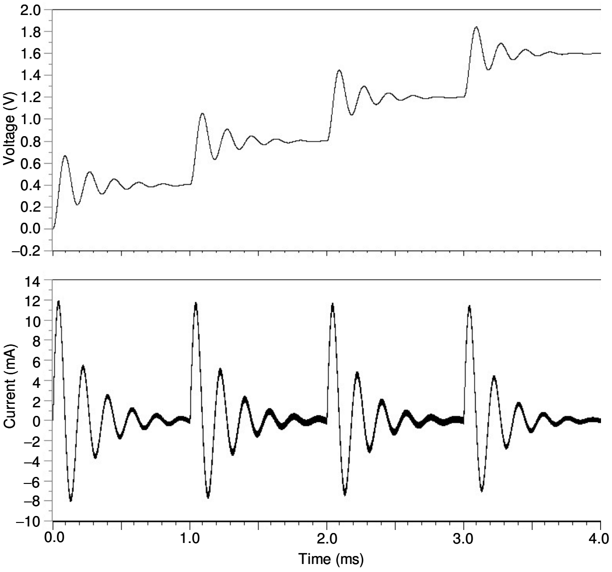

Fig. 5. *V* and *I* of step down converter when *L*=800 μH and *C*=1 μF.

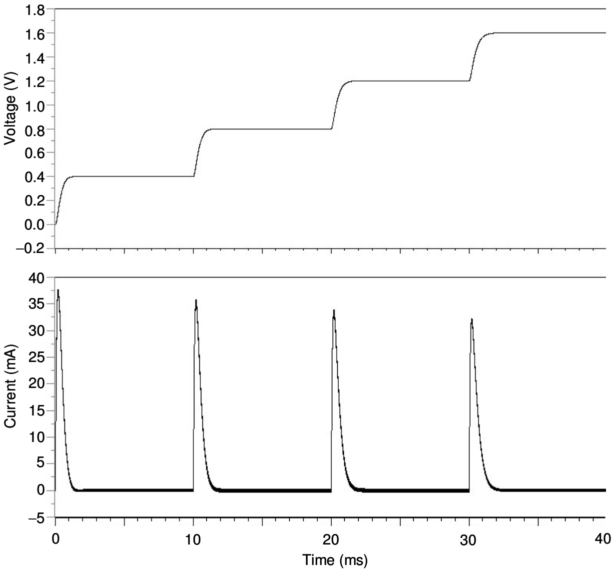

Fig. 6. *V* and *I* of step down converter when *L*=800 μH and *C*=50 μF.

time period for each step charging is 10 ms. In this case, the oscillation and the overshoot completely disappear. Regarding the current, it increases largely at the beginning and then decreases monotonically. This behavior is close to conventional *RC* circuit charging.

Due to the disappearance of the oscillation, when *C*=50 μF, $R^2-4L/C=0$ should be satisfied. Then, *R* is estimated to be 8 Ω. This value is consistent with the resistance of the switching transistor.

In the equilibrium state at *t*=19 ms, the current changes linearly between –0.3 and 0.3 mA. The –0.3 mA is also quite consistent with (6).

Now, we discuss the energy dissipation. Table I shows the power consumption *P* and the injected energy for charging the capacitor E_{inj} by the simulation. *L* is 800 μH and *C* is 20, 40, or 50 μF. The duty ratio is changed as 0.2, 0.4, 0.6, or 0.8. First, we discuss the situation when *d*=0.2 and

Table I. Power consumption and injected energy for charging the capacitor of step down converter when the duty ratio is changed stepwise.

d	*P* and E_{inj}		Simulation value		
		L	800μH		
		C	20 μF	40 μF	50 μF
0.2	Ave. *P* [mW] 0～10ms		0.342	0.660	0.819
	Ave. *P* [mW] 9～10ms		0.023	0.023	0.023
	E_{inj} for charging *C* [nJ]		3190	6370	7960
0.4	Ave. *P* [mW] 10～20ms		0.663	1.302	1.622
	Ave. *P* [mW] 19～20ms		0.024	0.024	0.024
	E_{inj} for charging *C* [nJ]		6390	12780	15980
0.6	Ave. *P* [mW] 20～30ms		0.983	1.942	2.422
	Ave. *P* [mW] 29～30ms		0.023	0.023	0.023
	E_{inj} for charging *C* [nJ]		9600	19190	23990
0.8	Ave. *P* [mW] 30～40ms		1.303	2.582	3.222
	Ave. *P* [mW] 39～40ms		0.023	0.023	0.023
	E_{inj} for charging *C* [nJ]		12800	25590	31900

C=20 μF. The average power consumption for *t*=0 to 10 ms is 0.342 mW. This value includes the power consumption of charging the capacitor and the steady power consumption of the circuit. The average power consumption for *t*=9 to 10 ms is 0.023 mW. We can confirm that the average power consumption for *t*=8 to 9 ms is also 0.023 mW. Therefore, it is concluded that 0.023 mW corresponds to the steady power consumption of the circuit. Then, we can estimate the injected energy for charging the capacitor E_{inj} during the first step. E_{inj} is consistent with the work done by the power supply. The total energy consumption during the first step is 3420 nJ. The steady energy consumption of the circuit during the first step is 230 nJ. Therefore, E_{inj} for charging the capacitor is 3190 nJ. The theoretical E_{inj} for charging the capacitor with constant power supply voltage dE is $dE\Delta Q$, where ΔQ is the stored charge difference in the capacitor. Then, when *d*=0.2, ΔQ is written as $0.2EC$. Therefore, $dE\Delta Q$ is calculated as 3200 nJ, which is consistent with the simulated value.

The simulated values for *d*=0.4, 0.6, and 0.8 are shown in Table I. Then, E_{inj} values for charging the capacitor are similarly calculated as 6390, 9600, and 12800 nJ for *d*=0.4, 0.6, and 0.8, respectively. The theoretical $dE\Delta Q$ values are 6400, 9600, and 12800 nJ, which are consistent with the simulated ones. Now, we consider the energy efficiency of stepwise adiabatic charging. The total E_{inj} for charging the capacitor is the sum of 3190, 6390, 9600, and 12800 nJ, which is 31980 nJ. The static electric energy of the capacitor is $CV^2/2$, which is calculated as $1/2 \cdot 20\mu F \cdot (1.6V)^2=25600$ nJ. The energy dissipation is the difference between the total E_{inj} for charging the capacitor and the capacitor's static electric energy. Therefore, the energy dissipation is 31980–25600=6380 nJ. In the conventional constant voltage charging, the energy dissipation is equal to $CV^2/2$, 25600 nJ. Then, the energy dissipation decreases to 6380/25600=24.9 %, which is consistent with the theoretical value of one-fourth for four-step charging. We can also confirm that energy dissipation decreases to one-fourth when *C*=40 and 50 μF.

Next, we consider the circuit with large load capacitance C_1 as shown in Fig. 7. Large capacitance of 100 μF is connected to the output voltage of the step down converter via resistor R_1. This circuit topology is conventionally used for the step down converter. The simulation of voltage and current is shown in Fig. 8. Here, *C* is set to 1 μF. While the

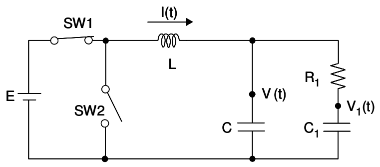

Fig. 7. Step down circuit with large load capacitance C_1.

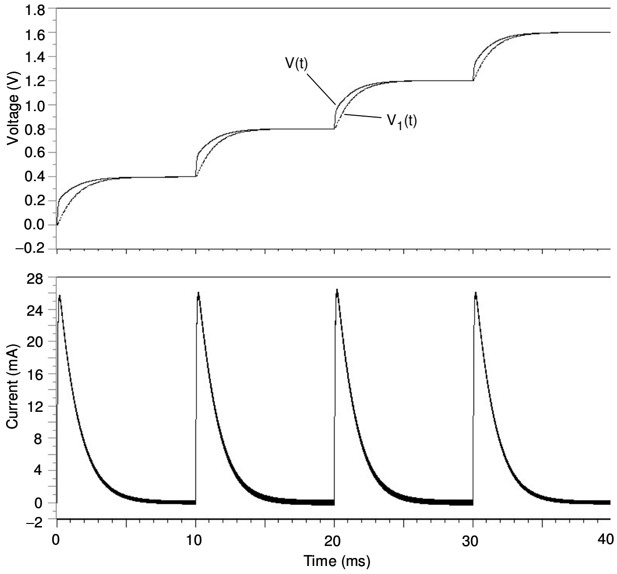

Fig. 8. V, V_1, and I of the circuit in Fig. 7. C and C_1 are 1 and 100 μF, respectively.

voltage in Fig. 5 oscillates largely, the voltage in Fig. 8 does not oscillate due to the large load capacitance, although these circuits have the same C of 1 μF.

Now, we consider the energy efficiency. Table II shows the simulation results in Fig. 8. When C=1 μF, E_{inj} values for charging the load capacitor are 16010, 32140, 48300, and 64360 nJ for d=0.2, 0.4, 0.6, and 0.8, respectively. The theoretical values are 16160, 32320, 48480, and 64640 nJ, which are consistent with the simulated ones. Now, we consider the energy efficiency of stepwise adiabatic charging. The total E_{inj} for charging the load capacitor is 160810 nJ. The $CV^2/2$ is calculated as 129280 nJ. Therefore, the energy dissipation of stepwise charging is 31530 nJ. As a result, the energy dissipation decreases to 31530/129280=24.4 %, which is consistent with the theoretical value of one-fourth. Similarly, we can confirm that, when C=10 μF, the energy dissipation decreases to 24.2 %, which is also consistent with the theoretical value.

In stepwise charging, energy efficiency is related to the number of steps. When we increase n, energy dissipation would become zero.

Here, we consider E_{inj} for charging the gate capacitance of SW1 and SW2 in Fig. 2(b) or Fig. 7. The simulation results are 0.7, 0.6, 0.6, 0.7 μW for d=0.2, 0.4, 0.6, and 0.8, respectively. The gate capacitance per area is 1 fF/ μm^2 so that the gate capacitance of SW1 is estimated to be 0.18·(100+200) fF=54 fF. Then, power consumption fCV^2 is calculated as $10^6 \cdot 54 \times 10^{-15} \cdot (3.3)^2 = 0.59$ μW. This value is consistent with the simulated value. From t=0 to 10 ms, the energy consumption of the SW1 gate is 5.9 nJ. This value is negligible compared with the 3190 nJ at C=20 μF in Table I or 16010 nJ at C=1 μF in Table II so that we can neglect E_{inj} of the gate capacitance.

Table II. Power consumption and injected energy for charging the capacitor in the circuit with large load capacitance of 100 μF.

d	P and E_{inj}		Simulation value	
		L	800μH	
		C	1 μF	10 μF
0.2	Ave. P (mW) 0～10ms		1.631	1.774
	Ave. P (mW) 9～10ms		0.030	0.032
	E_{inj} for charging C [nJ]		16010	17420
0.4	Ave. P (mW) 10～20ms		3.251	3.539
	Ave. P (mW) 19～20ms		0.033	0.037
	E_{inj} for charging C [nJ]		32140	35020
0.6	Ave. P (mW) 20～30ms		4.868	5.299
	Ave. P (mW) 29～30ms		0.038	0.045
	E_{inj} for charging C [nJ]		48300	52540
0.8	Ave. P (mW) 30～40ms		6.483	7.059
	Ave. P (mW) 39～40ms		0.047	0.058
	E_{inj} for charging C [nJ]		64360	70010

In Fig. 8, the period of the current peak is 10 ms so that the region of zero current is long. Of course, we can shorten the time period to 2 ms, in which the current does not decrease to zero and would go to the next peak. This charging method is good for high-speed operation. By decreasing the time period for step charging and increasing the step number, the stepwise charging becomes something close to constant current charging.

V. CONCLUSION

We investigated a step down converter with an inductor and capacitor analytically. From the analytical solution, it is derived that the voltage and current in the equilibrium state is dE and $d(1-d)TE/2L$, where d, E, T, and L are the duty ratio, power supply voltage, switching period, and inductance. Next, we discussed adiabatic stepwise charging, which is achieved by changing the duty ratio stepwise in the step down converter. Simulations clarified that the energy dissipation decreases to one-fourth when four-step charging is performed. The situation when there is large load capacitance was also simulated, and it is clarified that the energy dissipation decreases to one-fourth.

REFERENCES

[1] R. C. Merkle, "Reversible electronic logic using switches," *Nanotechnology,* vol. 4, no. 1, pp. 21–40, Jan. 1993.

[2] L. J. Svensson and J. G. Koller, "Driving a capacitive load without dissipating fCV^2," in *Proc. IEEE Symp. Low Power Electron.*, 1994, pp. 100–101.

[3] W. C. Athas, "Energy-Recovery CMOS," in *Low Power Design Methodologies*, J. M. Rabey and M. Pedram, Ed. Massachusetts: Kluwer Academic Publishers, 1996, pp. 65–100.

[4] S. Nakata, "Adiabatic charging reversible logic using a switched capacitor regenerator," *IEICE Trans. Electron.,* vol. E87-C, no. 11, pp. 1837–1846, Nov. 2004.

[5] S. Nakata, H. Suzuki, R. Honda, T. Kusumoto, S. Mutoh, H. Makino, M. Miyama, and Y. Matsuda, "Adiabatic SRAM with a shared access port using a controlled ground line and step-voltage circuit," in *Proc. IEEE ISCAS*, 2010, pp. 2474–2477.

[6] S. Nakata, M. Miyama, and Y. Matsuda, "An adiabatic charging and discharging method with minimum energy dissipation for a variable-gap capacitor system," *IET Circuits, Devices and Systems*, vol. 4, no. 4, pp.301-311, July 2010.