Optimizing silicon avalanche photodiode fabricated by standard CMOS process for 8 GHz operation

Optimizing Silicon Avalanche Photodiode Fabricated by Standard CMOS Process for Sub-10 GHz Operation

Zul Atfyi Fauzan M. N., Koichi Iiyama, Ryoichi Gyobu, Takuya Hishiki and Takeo Maruyama
School of Electrical and Computer Engineering,
Kanazawa University,
Kanazawa 920-1192 Japan

Zul Atfyi Fauzan M. N.
Faculty of Electronic and Computer Engineering,
Universiti Teknikal Malaysia Melaka (UTeM),
76100 Melaka, Malaysia
zulatfyi@utem.edu.my

***Abstract*—Silicon avalanche photodiode (APD) was fabricated by standard 0.18 µm CMOS process. The current-voltage characteristic and frequency response was measured for the APD with and without guard ring. With the existent of guard ring around the perimeter of the diode junction, it shows a better performance for the maximum bandwidth but in contrast it shows lower in responsivity. For the first time, an optimizing of electrode spacing, detection area and the PAD size for RF probing shows an enhancement of the bandwidth. The detection area and the PAD size for RF probing are reduced to 10 x 10 µm² and 30 x 30 µm², respectively, to decrease the device capacitance, the spacing of interdigital electrode is narrowed to 0.84 µm to decrease carrier transit time, and by cancelling the carriers photo-generated in the deep layer and the substrate because the carriers are slow diffusion carriers. As a result, the maximum bandwidth of 8.0 GHz was achieved along with gain-bandwidth product of 280 GHz.**

Keywords—Silicon, CMOS, Photodiode, Avalanche photodiode

I. INTRODUCTION

Short-distance optical data transmission has been widely studied for realizing board-to-board and chip-to-chip high-speed data transmissions. In these applications, short wavelength vertical-cavity surface-emitting lasers (VCSELs) and silicon (Si) photodiodes (PDs) are used for low-cost system configuration. Si PDs fabricated by complementary metal oxide semiconductor (CMOS) process are promising optical devices for easy integration with electronic circuits without any process modification, and avalanche photodiode fabricated by CMOS process (CMOS-APD) has been developed for optical interconnection applications [1]–[3]. We have studied CMOS-APDs with interdigital electrode structure for high-speed data transmission systems [4], [5] and for Blu-ray optical disc systems [6]. The CMOS-APDs with bandwidth over 1 GHz and the avalanche gain of more than 100 have been proposed and realized. We also reported 7 GHz-bandwidth CMOS-APD with the detection area of 20 x 20 µm², the electrode spacing of 1 µm and the PAD size for RF probing of 30 x 30 µm² [7]. Here we report a CMOS-APD with the maximum bandwidth was enhanced to 8.0 GHz bandwidth and the gain-bandwidth product of 280 GHz by narrowing the electrode spacing to 0.84 µm, decreasing the detection area and the PAD size for RF probing to 10 x 10 µm² and 30 x 30 µm², respectively. The selected CMOS-APD also measured for with and without guard ring (GR) structure.

II. STRUCTURE

Fig. 1 shows the photograph of the fabricated CMOS-APD. It has two parts which are the detection area and the PAD for RF probing. The detection area which contains CMOS-APD is connecting to the three different PADs for voltage bias and ground. The detection area and the PAD size are S_{DT} = 20 x 20 µm² and S_{PAD} = 40 x 40 µm², respectively.

Fig. 2 shows the cross-sectional structure of the CMOS-APD fabricated by standard 0.18 µm CMOS process without process modification. The P-substrate, Deep Nwell (DNW), Pwell and shallow trench isolation (STI) oxide from standard process are used to implement the p-n diodes in this CMOS-

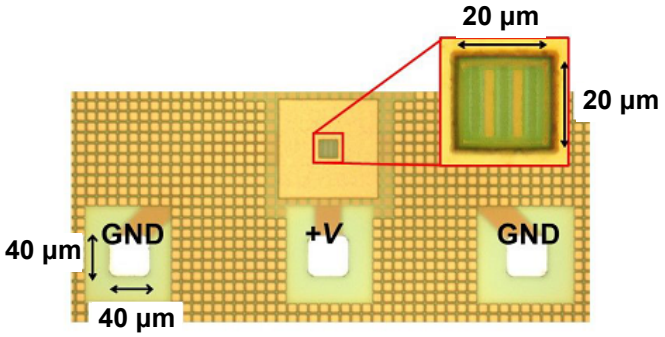


Fig. 1. Photograph of the fabricated CMOS-APD.

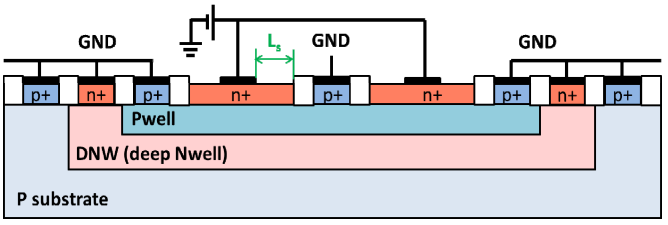


Fig. 2. Structure of CMOS-APD nMOS type fabricated by standard CMOS process.

APD design. STI oxide is used for forming isolation regions between active devices. The n^+- and p^+- layers are alternatively arranged and then the electrodes are interdigital structure with the electrode spacing, L_S = 1.00 µm. The light is illuminated from the top of the device.

From the figure, to recognize the different between CMOS-APD with and without GR structure is the connection of electrodes on P-substrate, DNW and Pwell to the ground. If all electrodes are electrically shorted, it represents the existence of a GR. If not, the structure is without a GR as we report here, the electrode on P-substrate and DNW are open. The addition of the GR at the junction perimeter is used to control leakage current under high bias.

The structure is the same with nMOS structure in a P-substrate so-called CMOS-APD nMOS type. As all electrodes are electrically shorted in CMOS-APD with GR, the photo-generated electrons in P-substrate and DNW will move towards n^+-layers on the DNW while photo-generated holes go through the p^+-layers on the P-substrate because of the built-in potential barrier between the P-substrate and the DNW. It is then recombined but do not contribute to the photocurrent. In the Pwell, the photo-generated electrons and holes are drifted towards the n^+-layers and p^+-layers, respectively.

For CMOS-APD without GR device, the potential barrier between DNW and Pwell that we cannot confirm but maybe low lead to the travel of photo-generated electrons and holes from P-substrate toward the n^+-layers and p^+-layers on the Pwell, respectively. It is happen due to both p^+-layers on the P-substrate and n^+-layers on the DNW are not electrically connected together to the ground. In this CMOS-APD, the photo-generated electrons are efficiently multiplied due to avalanche mechanism because a high electric field is applied around the interface between the n+-layers and Pwell.

III. Characterization

Fig. 3 shows the successfully plotted I-V characteristic from the measurement of CMOS-APD n-MOS type included with and without guard ring. The dark current at a low bias is about 10 pA, and the breakdown voltage measured when the dark current exceeds 1 µA is about 9.05 V. Under light illumination at 20 µW, the photocurrent relatively constant with the increasing reverse bias voltage, but then it gradually increased above 4.0 V until it reaches the maximum value at the breakdown voltage. The current is significantly increased before breakdown voltage due to avalanche amplification.

Fig. 4 shows the responsivity of the fabricated CMOS-APD with and without guard ring as a function of the reverse bias voltage. The responsivity, which is the ratio of the photocurrent to the optical power was obtained from Fig. 3 but take into account the input optical power of 10 µW and 30 µW. Responsivity increases initially with the reverse bias voltage because of the depletion width increased. It is then dramatically increases above 7.0 V due to avalanche amplification and finally the maximum responsivity was achieved at 9.05 V bias voltage. The responsivity of CMOS-APD with GR is lower than that of without GR because the quantum efficiency decreased due to connection of electrodes on P-substrate, DNW and Pwell to the ground.

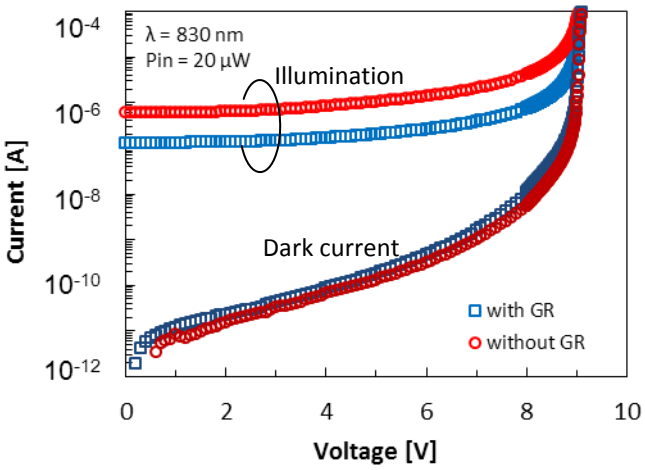


Fig. 3. I-V characteristics of the fabricated CMOS-APD nMOS type included with and without guard ring.

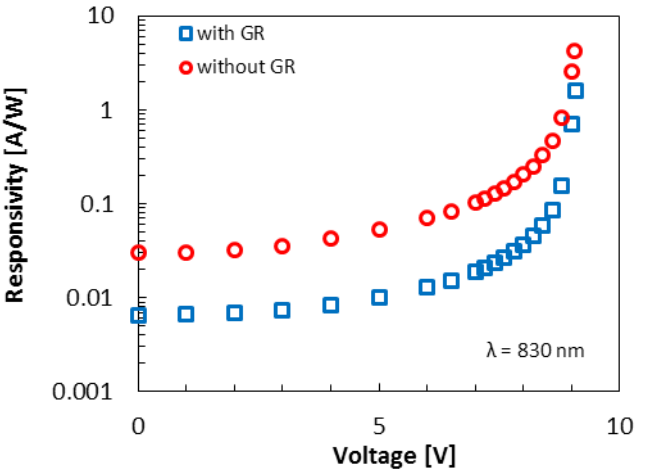
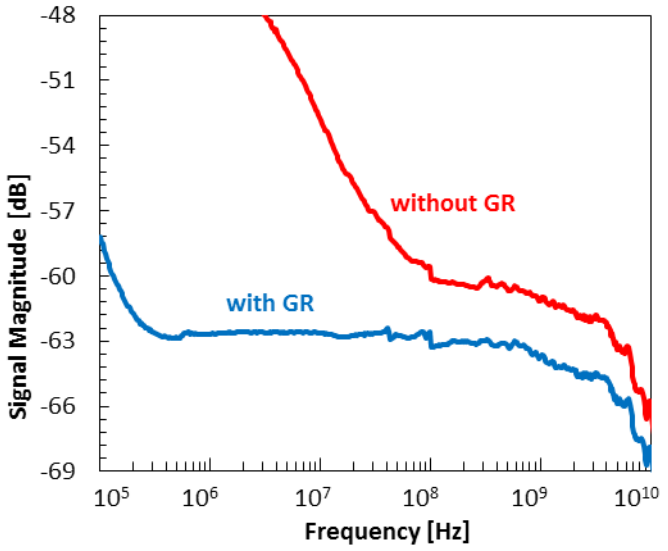
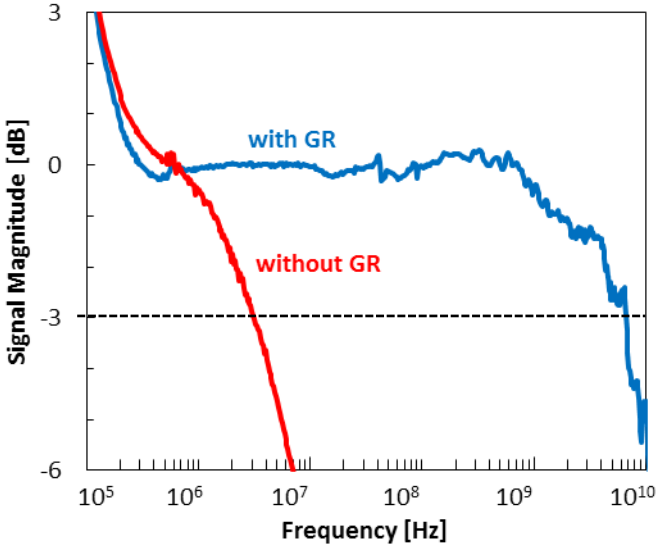


Fig. 4. Measured responsivity of the fabricated CMOS-APD nMOS type included with and without guard ring.

Fig. 5 shows the frequency response of CMOS-APD nMOS type with consideration of a GR and without GR. In the measurement, a laser light with the wavelength of 850 nm was intensity modulated by VCSEL with the bandwidth up to 10 GHz. The frequency response of the VCSEL and RF cables are compensated by using a commercial GaAs PIN photodiode with the nominal bandwidth of 30 GHz (Albis Optoelectronics AG, PQW30A-S). Two type of network analyzer was used to measure the frequency response for low frequency 100 kHz to 1.8 GHz (Hewlett Packard 4396A) and high frequency 10 MHz to 20 GHz (Agilent Technology E8 363B). Refer to Fig. 5(a), the frequency response for CMOS-APD without GR is too slow compared to with GR drastically at low frequency because the carriers photo-generated in the deep layer and the substrate are slow diffusion carriers. Refer to 3-dB frequency response in Fig. 5(b), the maximum bandwidth for CMOS-APD with GR is wider for about three order compared to without GR due to decrease carrier transit time, and by cancelling the carriers photo-generated in the deep layer and the substrate because the carriers are slow diffusion carriers.



(a)



(b)

Fig. 5. (a) Measured and (b) 3-dB frequency responses of the fabricated CMOS-APD for 8.5 V reverse biased voltage at 850 nm wavelength.

IV. Optimization

In this part, we will prove the role of L_S, detection area and PAD size which can optimize the bandwidth performance by doing an investigation on CMOS-APD nMOS type with GR. The bandwidth can be enhanced with decreasing the electrode spacing L_S due to decrease carrier transit time. It is also done by decreasing the detection area and the PAD size for RF probing due to decreased depletion capacitance and the PAD capacitance, respectively. Thus, we fabricated the CMOS-APD with the electrode spacing L_S = 0.84 µm, 1.00 µm, 1.52 µm, 2.40 µm and 4.12 µm, the detection area S_{DT} = 10 x 10 µm², 20 x 20 µm², 30 x 30 µm², 40 x 40 µm² and 50 x 50 µm² and the PAD size for RF probing S_{PAD} = 30 x 30 µm², 40 x 40 µm², 50 x 50 µm², 60 x 60 µm², 70 x 70 µm² and 100 x 100 µm².

Fig. 6 shows the relationship between the bandwidth and the electrode spacing. With the varying of electrode spacing, the detection area and PAD size is 20 x 20 µm² and 40 x 40 µm², respectively. The bandwidth is maximized when the avalanche gain is about 10, and the maximum bandwidth of 7.0 GHz is achieved for the electrode spacing L_S = 0.84 µm. It can be discovered that, the more narrow the electrode spacing, the higher bandwidth can be achieved, but it have to be limited since the electrode spacing L_S = 1.00 µm shows similarly in that range.

Furthermore, the correlation between detection area and bandwidth should be taken into account. Fig. 7 shows the gain-bandwidth characteristics of CMOS-APD for different detection area. The electrode spacing and PAD size is 1.00 µm and 40 x 40 µm², respectively. The detection area of 10 x 10 µm² shows the largest bandwidth for about 8.0 GHz compared to other sizes. It means that, the smaller size of detection area can produce higher speed performance, however in this case, the detection area of 10 x 10 µm² probably the limit size to be shrunk due to density of the device.

Finally, an investigation related to the PAD size is shown in Fig. 8. The electrode spacing and detection area is 1.00 µm and 20 x 20 µm², respectively. We can prove that the larger size of PAD as large as 100 x 100 µm² with maximum bandwidth of 4.6 GHz will dropped the CMOS-APD bandwidth performance compared to PAD size as small as 30 x 30 µm² which result a maximum bandwidth of 7.0 GHz. This result also shows the smaller size of PAD for RF probing enhanced the maximum bandwidth. In spite of that, the PAD size have limitation to be small enough suitable for RF probe.

For AC gain more than 100, the relationship of the bandwidth and the AC gain can be approximated by a straight line, which is the product of the bandwidth and the AC gain indicates in a constant value so-called gain-bandwidth (GB) product. It is an index to represent the performance of the APD and the amplifier circuit. GB product for this CMOS-APD is 280 GHz.

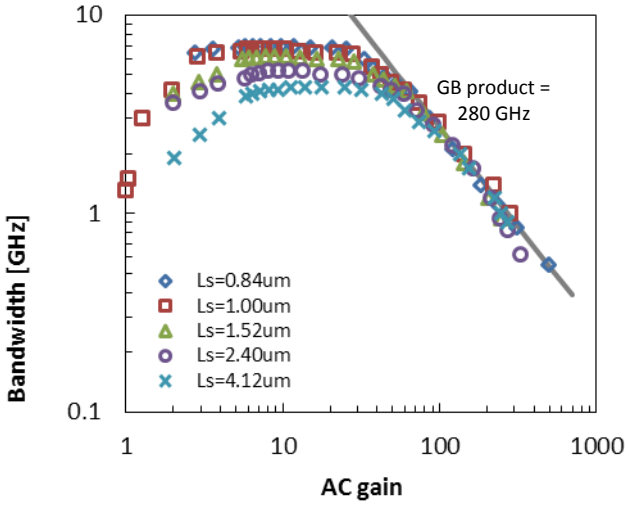


Fig. 6. Gain-bandwidth characteristics of CMOS-APD for various electrode spacing, L_S.

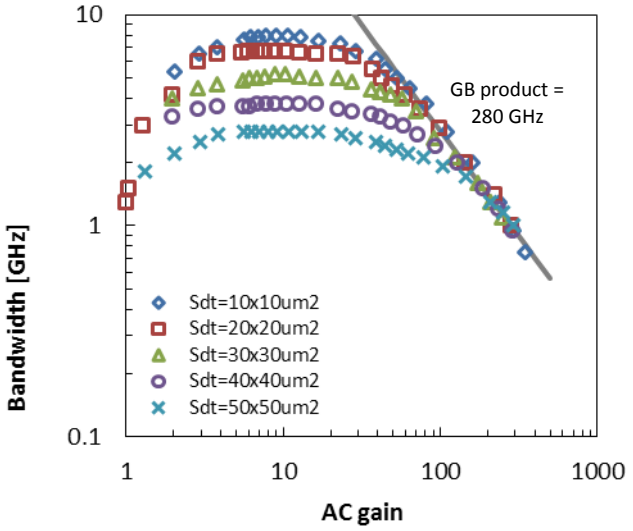


Fig. 7. Gain-bandwidth characteristics of CMOS-APD for various detection area.

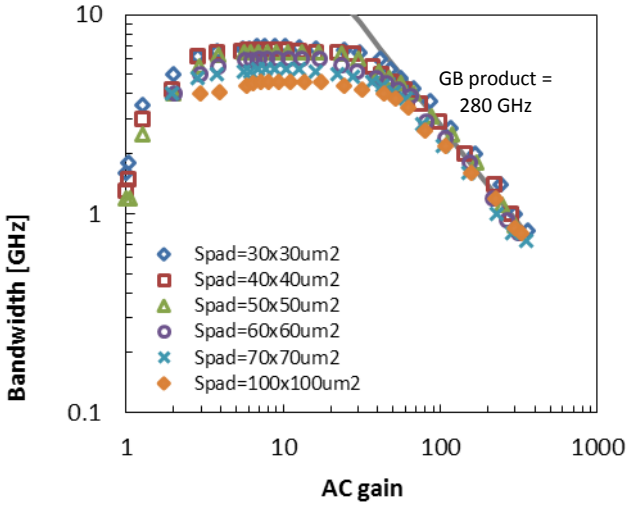


Fig. 8. Gain-bandwidth characteristics of CMOS-APD for various PAD size.

V. Conclusion

The CMOS-APD nMOS type with and without guard ring are fabricated by standard 0.18 µm CMOS process without process modification. In conjunction with the theory, this CMOS-APD shows a trade-off between the speed of response and quantum efficiency. The responsivity of CMOS-APD with GR is lower than that of without GR because the quantum efficiency decreased due to connection of electrodes on P-substrate, DNW and Pwell to the ground. Therefore, the maximum bandwidth for CMOS-APD with GR is wider compared to without GR due to decrease carrier transit time, and by cancelling the carriers photo-generated in the deep layer and the substrate because the carriers are slow diffusion carriers. By optimizing the electrode spacing to 0.84 µm, decreasing the detection area and the PAD size for RF probing to 10 x 10 µm² and 30 x 30 µm², respectively, the maximum bandwidth of a CMOS-APD was enhanced to 8.0 GHz with GB product of 280 GHz.

Acknowledgment

The CMOS-APD has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo, in collaboration with Rohm Corporation and Toppan Printing Corporation.

References

[1] W.-K. Huang, Y.-C. Liu, and Y.-M. Hsin, “A High-Speed and High-Responsivity Photodiode in Standard CMOS Technology,” IEEE Photonics Technol. Lett., vol. 19, no. 4, pp. 197–199, Feb. 2007.

[2] H.-S. Kang, M.-J. Lee, and W.-Y. Choi, “Si avalanche photodetectors fabricated in standard complementary metal-oxide-semiconductor process,” Appl. Phys. Lett., vol. 90, no. 15, p. 151118, 2007.

[3] M.-J. Lee and W.-Y. Choi, “A silicon avalanche photodetector fabricated with standard CMOS technology with over 1 THz gain-bandwidth product.,” Opt. Express, vol. 18, no. 23, pp. 24189–94, Nov. 2010.

[4] K. Iiyama, N. Sannou, and H. Takamatsu, “Avalanche Amplification in Silicon Lateral Photodiode Fabricated by Standard 0 . 18 µ m CMOS Process,” no. 11, pp. 1820–1823, 2008.

[5] K. Iiyama, H. Takamatsu, and T. Maruyama, “Hole-Injection-Type and Electron-Injection-Type Silicon Avalanche Photodiodes Fabricated by,” vol. 22, no. 12, pp. 932–934, 2010.

[6] T. Shimotori, K. Maekita, T. Maruyama, and K. Iiyama, “Characterization of APDs fabricated by 0 . 18 m CMOS process in blue wavelength region,” no. July, pp. 0–1, 2012.

[7] T. Shimotori, K. Maekita, R. Gyobu, T. Maruyama, and K. Iiyama, “Optimizing interdigital electrode spacing of CMOS APD for 10 Gb / s application,” pp. 6–7.