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Research Article

Circuit Implementation, Operation, and Simulation of Multivalued Nonvolatile Static Random Access Memory Using a Resistivity Change Device

Kazuya Nakayama[1] and Akio Kitagawa[2]

[1] *Faculty of Medicine, Graduate School of Medical Science, Kanazawa University, 5-11-80, Kodatsuno, Kanazawa 920-0942, Japan*
[2] *Faculty of Engineering, Graduate School of Natural Science & Technology, Kanazawa University, Kakuma, Kanazawa 920-1192, Japan*

Correspondence should be addressed to Kazuya Nakayama; knaka@kenroku.kanazawa-u.ac.jp

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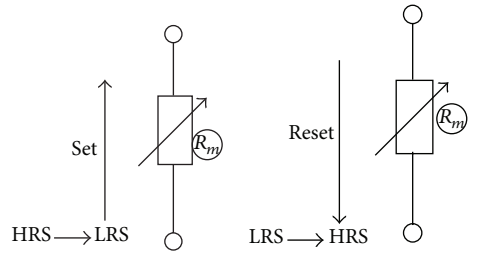
We proposed and computationally analyzed a multivalued, nonvolatile SRAM using a ReRAM. Two reference resistors and a programmable resistor are connected to the storage nodes of a standard SRAM cell. The proposed 9T3R MNV-SRAM cell can store 2 bits of memory. In the storing operation, the recall operation and the successive decision operation of whether or not write pulse is required can be performed simultaneously. Therefore, the duration of the decision operation and the circuit are not required when using the proposed scheme. In order to realize a stable recall operation, a certain current (or voltage) is applied to the cell before the power supply is turned on. To investigate the process variation tolerance and the accuracy of programmed resistance, we simulated the effect of variations in the width of the transistor of the proposed MNV-SRAM cell, the resistance of the programmable resistor, and the power supply voltage with 180 nm 3.3 V CMOS HSPICE device models.

1. Introduction

Power dissipation has been one of the most serious concerns in highly integrated CMOS logic circuits. For example, a leakage current's effect becomes dominant in the standby mode. One solution is to use nonvolatile memory, which has been proposed. Typical new types of memory include ferroelectric random access memory (FeRAM), magnetoresistive RAM (MRAM), phase change RAM (PRAM), and resistivity change RAM (ReRAM). A nonvolatile SRAM (NV-SRAM) has also been developed to mitigate restriction in program cycles and to improve the access time [1–5]. The component count of the NV-SRAM is large because the nonvolatile portion must be added to the SRAM portion.

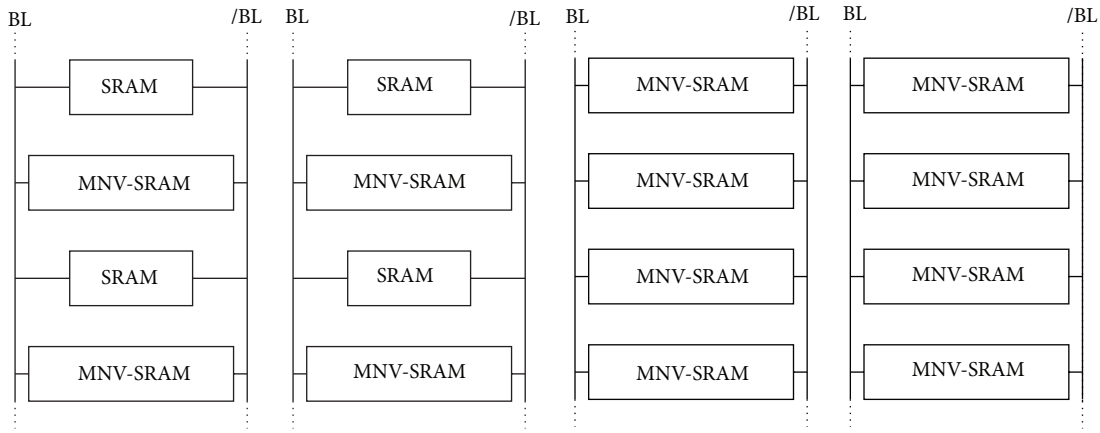
The large resistivity change of ReRAM and PRAM is a superior characteristic and has been studied for multivalued nonvolatile memory [6–10]. For example, 16 separate states for multivalued storage were reported in [6]. ReRAM has been widely expected for use as the next generation of nonvolatile memory because of its superior characteristics, such as low-voltage operation, high-speed performance, and low power. This device has two switching modes: (i) unipolar switching, in which the device depends on the pulse width and amplitude of the applied voltage, and (ii) bipolar switching, in which the device depends on the polar character. In this paper, we used a bipolar switching device that made the best use of this proposed circuit. Figure 1 shows the definition of the set and reset operations for the bipolar switching device. Set is defined as an operation conducted to change from a high resistance state (HRS) to a low resistance state (LRS), and reset is an operation to change from LRS to HRS.

In this paper, we apply the multivalued storage technology to the NV-SRAM. The proposed multivalued nonvolatile SRAM (MNV-SRAM) can hold 2 bits (4 values) of memory in standby mode and acts as conventional SRAM in a normal (SRAM) operation. By replacing half of the conventional SRAM array with MNV-SRAM cells, NV-SRAM memory is realizable, as shown in Figure 2(a). The number of elements (transistor and resistor) required to hold 1 bit can be reduced using the proposed MNV-SRAM cells. Furthermore, when



(a) Set operation (b) Reset operation

Figure 1: Current flow of the set and reset operations of ReRAM (bipolar switching device).



(a) SRAM + MN-VSRAM array (b) MNV-SRAM array

Figure 2: Array structure. (a) Half of the array is SRAM. (b) All of the array is MNV-SRAM.

all of the cells are replaced with MNV-SRAM cells, as shown in Figure 2(b), the capacity becomes twice that of the conventional memory. We also propose a stable recall operation. The recall operation of conventional NV-SRAM with the programmable resistor is not very stable. It will become even more unstable since process variations increase along with the progress of scaling in CMOS technology.

In this paper, we describe the cell's design and operation. We also present the results from the HSPICE simulation of the proposed MNV-SRAM cell using a 180 nm 3.3 V CMOS device model.

2. Cell Structure and Operation

Figure 3 outlines the circuit topologies of conventional NV-SRAM and the proposed MNV-SRAM. The former 8 transistor 2 resistor (8T2R) cell is an improved cell for the conventional shadow RAM [1, 2] and has been applied to magnetic tunnel junctions (MTJs) [4]. The latter 9 transistor 3 resistor (9T3R) cell, which is added to the former 1 resistor (R_{refb}) and 1 transistor (M9), also consists of standard SRAM portions and the nonvolatile memory portion. R_{ref}, R_{refa}, and R_{refb} are fixed reference resistors and R_m is a programmable resistor. These reference resistors and the programmable resistor are connected to the storage node (S1 and S2) of a standard SRAM cell.

The proposed MNV-SRAM cell has two reference resistors (R_{refa} and R_{refb}). By having two reference resistors, the reference resistance can be changed to three values, R_{refa}, R_{refb}, and the parallel resistance of R_{refa} and R_{refb} ($R_{\text{refa}}//R_{\text{refb}}$) as shown in Figure 4. For example, the reference resistance can be changed into 100 kΩ, 65 kΩ, and 39 kΩ, when R_{refa} and R_{refb} are set to 100 kΩ and 65 kΩ, respectively. Therefore, 4 values (2 bits) can be determined as shown in Figure 4(b). It is not necessary to prepare three reference resistances (R_{refa}, R_{refb}, and R_{refc}). The resistance of R_m depends on material (composition), size, and write/erase pulse conditions. It is necessary to define R_{refa} and R_{refb} according to the resistance distribution of R_m. For simplicity, in this paper, it is assumed that the distribution of R_m is uniform from 0 to 150 kΩ and R_{refa} and R_{refb} are assumed to be fixed resistors which used high resistance polysilicon, and so forth.

The operation scheme, associated with control signals, and main current flows for the proposed MNV-SRAM are outlined in Figure 5. In order to read 2-bit information, the read operation is performed twice in the recall operation. The SRAM + MNV-SRAM array (Figure 2(a)) is used for introduction to the recall operation, and R_{refb} is smaller than R_{refa}. The store operation is also introduced in this paper.

2.1. Recall Operation. It is assumed that R_m stores (holds) 4 values (2 bits) in this paper. In the first recall operation,

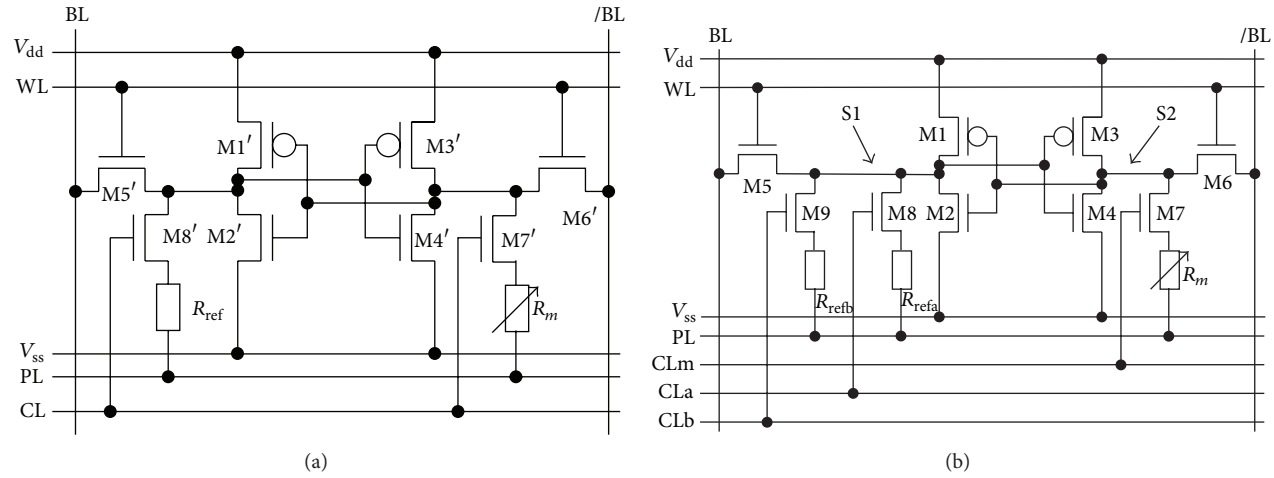


Figure 3: (a) Conventional NV-SRAM cell and (b) proposed MNV-SRAM.

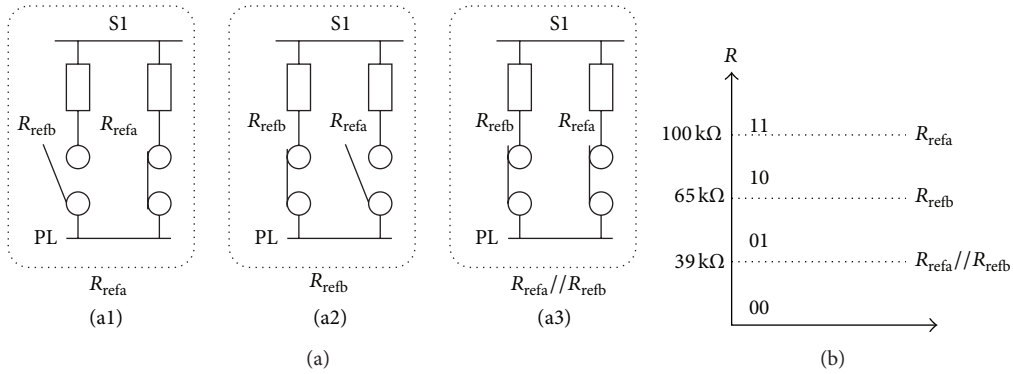


Figure 4: Reference resistances.

CLm, CLa, and CLb are set to "H," "L," and "H," respectively (M7 and M9 are turned on and M8 is turned off). Therefore, R_m can be compared to R_{refb} (Figure 4(a2)). During recall, transistors M7 and M9 are turned on. A certain current (or voltage) is applied from the precharge circuit (i) before/Cpm is set to the "L" state. The voltage of nodes S1 (V(S1)) and S2 (V(S2)) in Figure 5(a) increases depending on R_{refb} and R_m. When R_{refb} is larger than R_m, V(S1) is lower than V(S2). Therefore, the information stored in R_m can be recalled into the SRAM portion of MNV-SRAM after/Cpm is set to the "L" state (when the power supply for the cell is turned on). Then, the recalled data is moved from MNV-SRAM to SRAM using read and write circuits. The high-order bit is read out in this process.

In the second recall operation, both CLm and CLa are set to "H." CLb depends on the results of the first recall operation. When R_m is smaller than R_{refb}, CLb is set to "H." R_m is compared to $R_{refa}//R_{refb}$ (Figure 4(a3)). On the other hand, when R_m is larger than R_{refb}, CLb is set to "L." R_m is compared to R_{refa} (Figure 4(a1)). The low-order bit is read out in this process.

This recall step and read-out of 2-bit data are shown in Figure 6.

2.2. SRAM Operation. Normal SRAM operations can be performed by closing transistors M7, M8, and M9, as shown in Figure 5(b).

2.3. Store Operation. Figures 5(c) and 5(d) outline the store operation, which is performed just before power off. The information stored in SRAM (high-order bit) and (SRAM part of) MNV-SRAM (low-order bit) in Figure 5(a) is read first. The reference resistor is selected by this read information. For example, when the read information is "01," R_m needs to be set between R_{refb} and $R_{refa}//R_{refb}$. When R_m is larger than R_{refb}, the set pulse needs to be applied to R_m. When R_m is smaller than $R_{refa}//R_{refb}$, the reset pulse needs to be applied to R_m as shown in Figure 7.

In order to compare R_m with R_{refb}, CLm, CLa, and CLb are set to "H," "L," and "H," respectively. Then, the recall operation is carried out. When R_m is larger than R_{refb}, node S2 is automatically set to "L" (0 V) in this recall operation. A set voltage (required for set operation) is applied from PL. After that, the set pulse is applied to R_m in order to make R_m have a lower resistance, as shown in Figure 5(c). On the other hand, when R_m is smaller than R_{refb}, the V(S2) is set to "H"

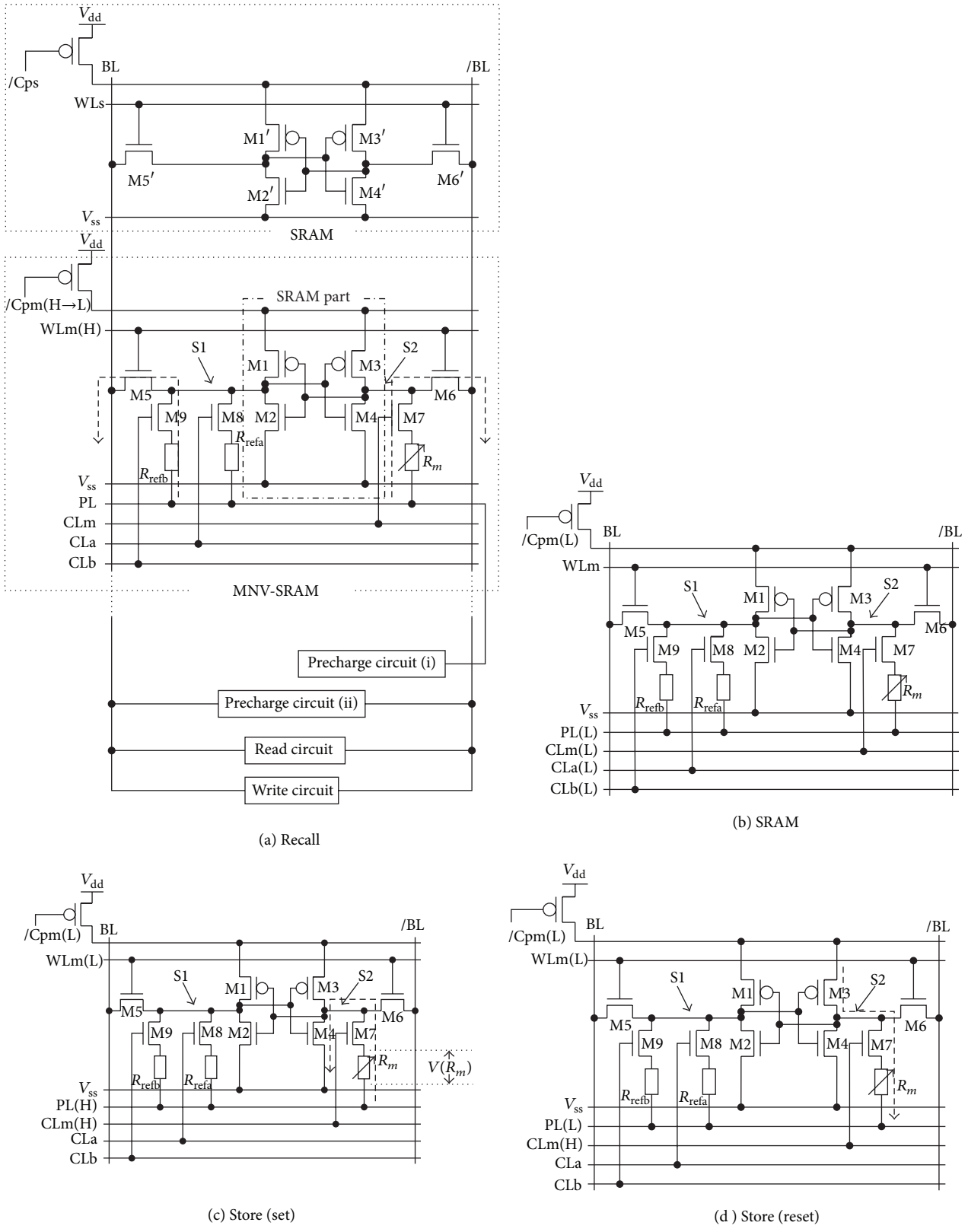


Figure 5: Operation scheme for MNV-SRAM.

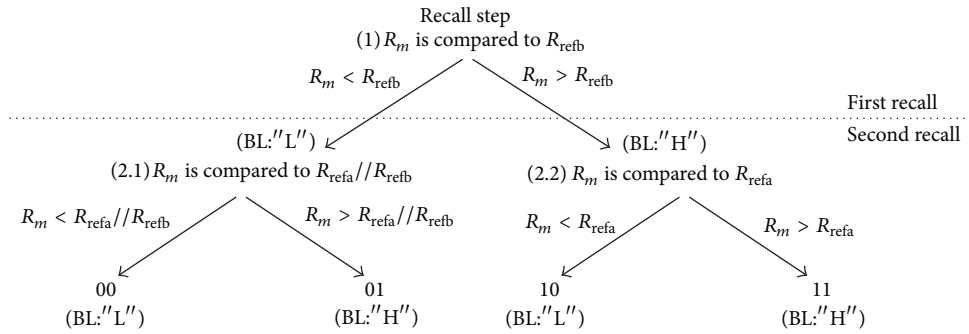


Figure 6: Recall step for MNV-SRAM.

Table 1: Relationship of R_m, nodes potential (S2 and PL), and applied pulse for the store operation.

		S2	PL	
First store	$R_m > R_{refb}$	L	H	Set pulse
	$R_m < R_{refb}$	H	H	—
Second store	$R_{refa}//R_{refb} < R_m$	L	L	—
	$R_{refa}//R_{refb} > R_m$	H	L	Reset pulse

Table 2: ReRAM device characteristics [11].

Set voltage	More than 2.2 V
Set transition time	~50 ns
Reset voltage	Less than −1.4 V
Reset transition time	~50 ns

automatically. The current which flows through R_m is zero (or a small value) because the voltage of both ends of R_m is high (H).

Next, all of CLm, CLa, and CLb are set to "H" and the recall operation is carried out. R_m is compared to $R_{refa}//R_{refb}$. When R_m is smaller than $R_{refa}//R_{refb}$, node S2 is set to "H" automatically in this recall operation. Then, the PL is set to low voltage (or 0 V). The reset pulse is applied to R_m, as shown in Figure 5(d). On the other hand, when R_m is larger than $R_{refa}//R_{refb}$, node S2 is set to "L" automatically. The current that flows through R_m is zero (or a small value) because the voltage of both ends of R_m is low.

The write pulse is not applied to R_m when the value of R_m is between $R_{refa}//R_{refb}$ and R_{refb} by using this method. The current flow directions of store (reset) and store (set) are opposite, as shown in Figures 5(c) and 5(d).

Table 1 shows the relationship of R_m, the nodes potential (S2 and PL), and the applied pulse.

3. Simulation

3.1. Simulation Condition. The device characteristics of the ReRAM are assumed in Table 2 [11]. These data are the set/reset conditions for a single-level cell using CoOx [11]. The resistance of the set state was 5 kΩ and the resistance of the reset state was reported to be within 10 kΩ and 150 kΩ. Then, it was assumed that R_m changes from 10 kΩ to 150 kΩ, and the set and reset voltages were assumed to be lower than the values shown in Table 2. 1024 cells were connected in a bit line (BL), as shown in Figure 2. Here, peripheral control circuits, such as address decoding and timing generation, are not included in our simulation condition. The wiring capacity and the wiring resistor are not included, either. The simulation conditions are listed in Table 3.

Table 3: Simulation condition.

Simulator	HSPICE
Fabrication process	180 nm CMOS
Power supply	3.3 V
Temperature	300 K

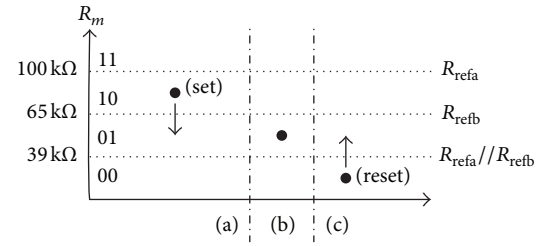


Figure 7: Write pulse required when "01" is stored in R_m.

3.2. Recall Operation. Figures 8 and 9 show the simulation results for the recall operation. R_{refa} and R_{refb} were fixed at 100 kΩ and 65 kΩ, respectively. In this case, the reference resistances R_{refa}, R_{refb}, and $R_{refa}//R_{refb}$ are 100 kΩ, 65 kΩ, and 39 kΩ, respectively.

First, /Cpm was set to "H" and nodes S1 and S2 were charged once by 0 V. Voltage (current) was applied to the BL, /BL, and PL using the precharge circuit (i) and (ii). A recall pulse of 600 mV was produced from the precharge circuit (i) (at 41 ns). When R_m was 50 kΩ, the voltage nodes S1 and S2 at 65 ns were 350 mV and 570 mV, respectively. The difference voltage V_{dl} (= V(S1) − V(S2) at 65 ns) was −220 mV. Since the voltage of node S1 was lower than that of node S2, after /Cpm was set to "L" (at 66 ns), nodes S1 and S2 could be set to "L" and "H," respectively. Next, this recalled data was moved from MNV-SRAM to SRAM using read and write circuits.

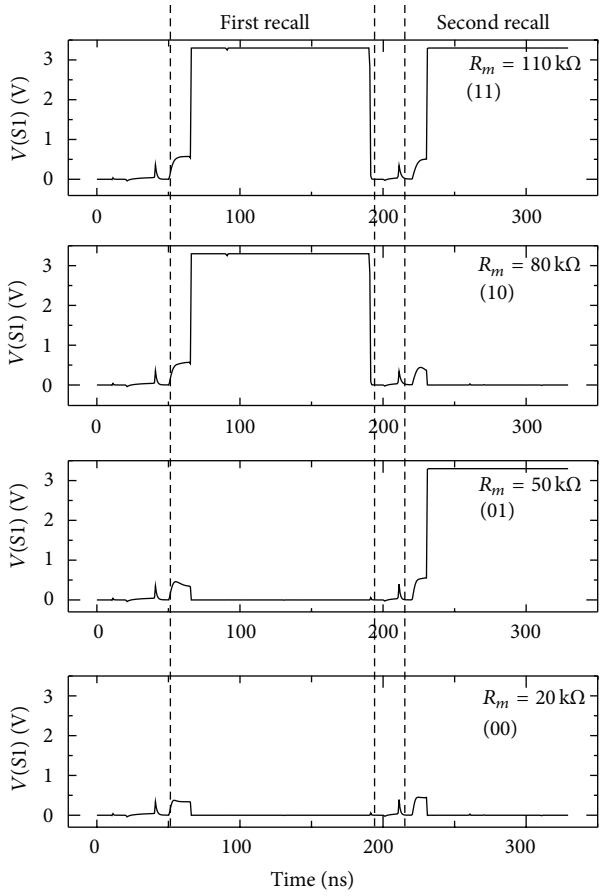


Figure 8: Simulation results for the recall operation. R_{refa} and R_{refb} were fixed at 100 and 65 kΩ, respectively.

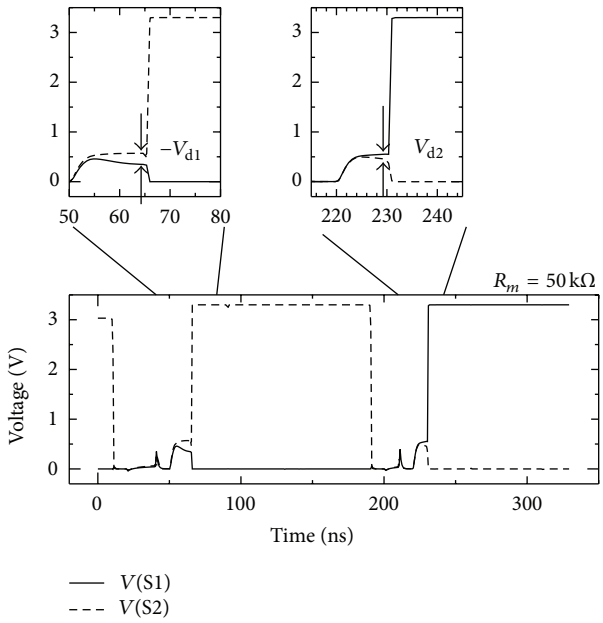


Figure 9: Simulation results for the recall operation. R_m, R_{refa}, and R_{refb} were fixed at 50, 100, and 65 kΩ, respectively.

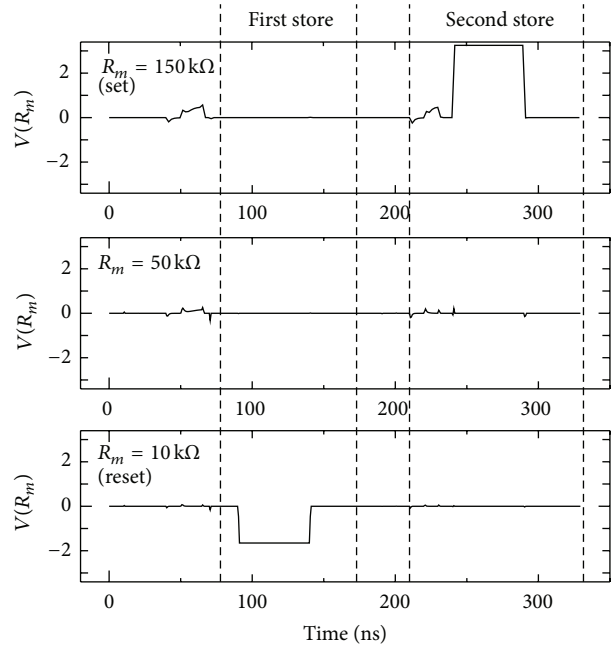


Figure 10: Simulation results for store operation. R_{refa} and R_{refb} were fixed at 100 and 65 kΩ. In this case, the information "01" was stored in R_m.

Second, /Cpm was set to "H" and nodes S1 and S2 were again charged by 0 V. The recall pulse of 600 mV was applied to the BL and /BL using the precharge circuit at 220 ns. When R_m was 50 kΩ, the voltage nodes S1 and S2 at 229 ns were 550 mV and 460 mV, respectively. The difference voltage V_{d2} (= V(S1) − V(S2) at 229 ns) was 90 mV. Since the voltage of node S1 was higher than that of node S2, after /Cpm was set to "L" (at 230 ns), nodes S1 and S2 could be set to "H" and "L," respectively. Therefore, when R_m is 50 kΩ, the information "01" is recalled in this way.

3.3. Store Operation. When the information "01" is stored in R_m, R_m needs to be set between 65 kΩ (= R_{refb}) and 39 kΩ (=R_{refa}//R_{refb}). There are three cases for the store operation, as shown in Figure 7. Figure 10 shows the simulation results for this store operation. It was confirmed that the circuits operated when the value of R_m was from 10 kΩ to 150 kΩ. When R_m was 150 or 10 kΩ, the set or reset pulse was applied to R_m, respectively. On the other hand, when R_m was 50 kΩ, the electric pulse did not need to be applied to R_m. The recall operation and the decision operation of whether or not the write pulse is required could be performed simultaneously. Therefore, the decision operation and circuit are not required when using this proposed scheme.

4. Discussion

4.1. Number of Elements of the Proposed Cell. Conventional MNV-SRAM cells consist of 8T2R, as shown in Figure 3(a) [1, 2, 4]. The proposed MNV-SRAM cell can hold 2 bits (4 values) of memory in standby mode by adding 3T3R to a

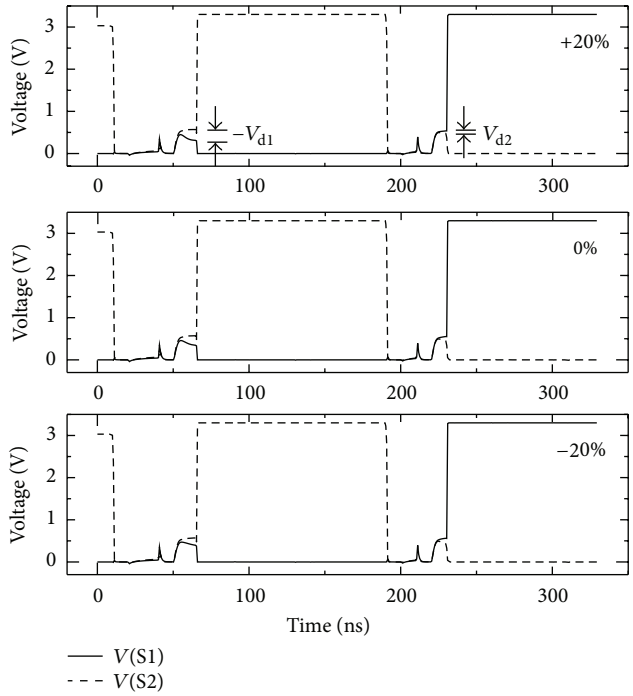


Figure 11: Effect of the channel width of the transistor on recall. Width of the channel of transistor M2 in Figure 3(b) varied from −20% to +20%. R_{refa}, R_{refb}, and R_m were fixed at 100, 65, and 50 kΩ, respectively.

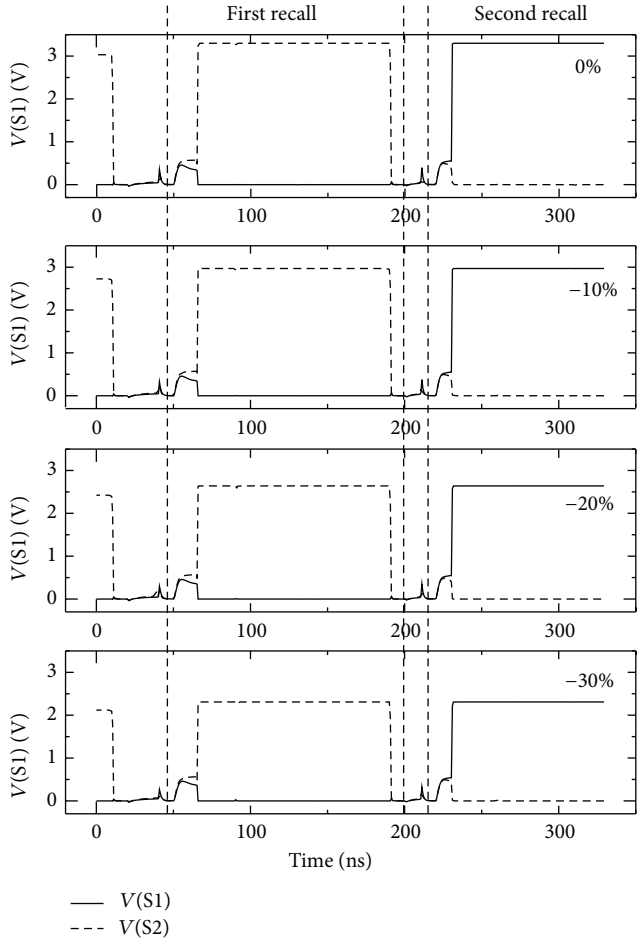


Figure 12: Effect of fluctuations on power supply voltage. Power supply voltage varied from −30% to 0%.

SRAM (6T) cell. In the array structure shown in Figure 1(a), 2 bits are recorded in 2 cells (SRAM + MNVSRAM, 6T + 9T3R). Therefore, the average number of elements required in order to memorize 1 bit of memory (ANE) is 7.5T1.5T, using the proposed MNV-SRAM cell. By using the proposed cell, the number of elements per cell can be reduced by 0.5T0.5R.

If the number of reference resistors is increased, a cell can memorize much more information theoretically. For example, the cell with three reference resistors can encode 3 bits/cell, and the cell with four reference resistors can memorize 4 bits/cell. Therefore, ANE decreases with an increase in the quantity memorized per cell, as shown in Table 4. However, a read/write margin rapidly decreases with an increase in the quantity memorized per cell.

4.2. Recall Stability. One of the most serious problems with MNV-SRAM is the stability of recall. The data integrity of the proposed MNV-SRAM cell is dominated by recall since all resistance information must be properly regenerated to the corresponding SRAM and SRAM portion of MNV-SRAM. The recall operation is used also for the store operation. The effect of variations in device characteristics (device mismatch) on recall is described below. Figure 11 plots the effect of the channel width of the transistor on recall. For simplicity, we have only shown that the width of the channel of NMOS transistor M2 in Figure 3(b) varied by 20%. R_{refa}, R_{refb}, and R_m were fixed at 100, 65 and, 50 kΩ, respectively. For example, when the width is narrowed by −20%, the V_{dl} decreases (−220 mV (0%) → −174 mV (−20%)) at 65 ns. However,

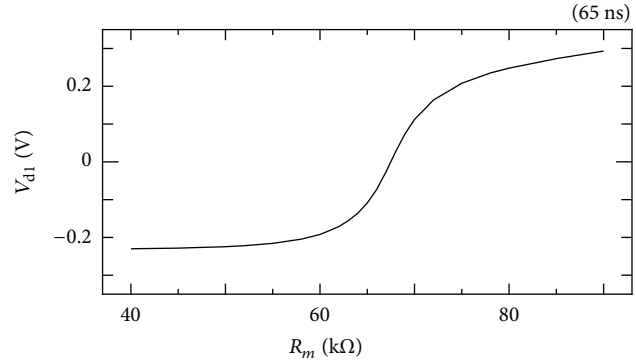
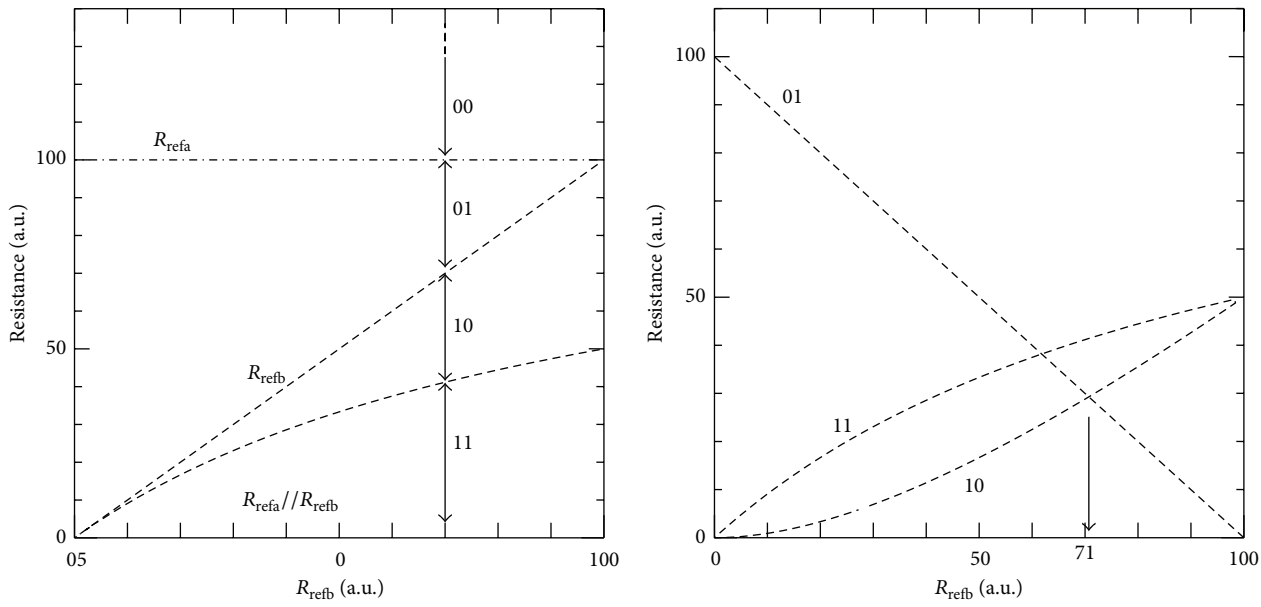


Figure 13: Effect of R_m fluctuations. V_{dl} shows the different voltage between the node S1 and S2 ($V_{dl} = V(S1) - V(S2)$). R_m was compared to R_{refb}, and R_{refb} was fixed at 65 kΩ. R_m varied from 40 to 90 kΩ.

the V_{d2} increases slightly (90 mV (0%) → 115 mV (−20%)) at 229 ns. In all cases, the recall operation was performed correctly. However, the precharge operation is not used in the conventional recall operation [4]. The recall operation easily malfunctions without the precharge operation. For example,



(a) Reference resistances

(b) Margins of reference resistances

FIGURE 14: (a) Reference resistances. R_{refa} is fixed and R_{refb} is changed from 0 to 100. $R_{refa}//R_{refb}$ shows the parallel resistance of R_{refa} and R_{refb}. (b) The difference between reference resistances (the amount of margins separating the states). 01 shows the difference between R_{refa} and R_{refb} ($R_{refa} - R_{refb}$). 10 shows "$R_{refb} - R_{refa}//R_{refb}$". 11 shows the value of $R_{refa}//R_{refb}$.

TABLE 4: The relation between the average number of elements required in order to memorize 1 bit (ANE) and the quantity memorized per cell (QMPC).

QMPC (bit/cell)	1	2	3	4
ANE	8 T 2 R	7.5 T 1.5 R	7.33 T 1.33 R	7.25 T 1.25 R

TABLE 5: Corner analysis of V_{d1} during first recall.

	NMOS		
	Slow	Typical	Fast
PMOS			
Slow	−30 mV	—	−480 mV
Typical	—	−220 mV	—
Fast	−30 mV	—	−470 mV

TABLE 6: Corner analysis of V_{d2} during second recall.

	NMOS		
	Slow	Typical	Fast
PMOS			
Slow	13 mV	—	380 mV
Typical	—	90 mV	—
Fast	14 mV	—	380 mV

if the width of NMOS transistor M2 is narrowed by 1%, the recall operation malfunctions without the precharge process.

Figure 12 shows the effects of power supply voltage fluctuations. The supply voltage varied from −30% to 0%. The recall operation was correctly executed for the supply voltage fluctuations. However, a drop in the supply voltage to −30% reduced the voltage difference to 30 mV (−220 mV → −190 mV at 65 ns).

Tables 5 and 6 list the dependencies of the V_{d1} and V_{d2} on transistor models. In this case, R_{refa}, R_{refb}, and R_m are fixed at 100, 65, and 50 kΩ, respectively. The V_{d1} and V_{d2} strongly depend on the characteristic of NMOS.

Figure 13 shows the effect of R_m fluctuations. V_{d1} showed different voltages between the nodes S1 and S2 ($V_{d1} = V(S1) - V(S2)$). R_m was compared to R_{refb}, and R_{refb} was fixed at 65 kΩ. R_m varied from 40 to 90 kΩ. The threshold resistance was 67 kΩ and it was a little bigger than R_{refb}. It seems that the threshold resistance shifted, since the number of resistors (FETs) connected to S1 (R_{refa} and R_{refb}) and S2 (R_m) differed. The recall operation is easy when the absolute value of V_{d1} is large. If the absolute value of V_{d1} must be 100 mV or more, R_m must be smaller than 65 kΩ or larger than 70 kΩ in this study. If the circuits are optimized, these points could improve.

4.3. Reference Resistor. In order to enlarge a read margin, it is necessary to enlarge the reference resistance differences. Figure 14 shows the reference resistances and the differences between the reference resistances. R_{refa} was fixed at 100 and R_{refb} was changed from 0 to 100. The differences of the reference resistances reached a maximum by $R_{refa}^2 = 2R_{refb}^2$. For example, the values of R_{refa} and R_{refb} were set to 100 kΩ and 71 kΩ, respectively. Then, the value of $R_{refa}//R_{refb}$ was set to 42 kΩ.

4.4. Energy Break Even Time. The energy break even time (EBT) [12] is also important for MNV-SRAM. The EBT

depends on write/recall energy, the leakage current of FETs, and so forth. However, it is difficult to estimate the EBT because the energy-consuming write/verify cycles are usually required in multivalued nonvolatile memory. Therefore, the EBT also depends on the number of write/verify cycles. Although it was a rough estimate, we estimated the EBT by the following easy model. (i) The set/reset condition in [11] (Table 2) and its behavior model [13] were used. (ii) The write energy was assumed to be the average of set and reset energy as reported by Kawabata et al. [11]. (iii) Write and recall cycles were only one cycle each and the verifying cycle was zero. It was estimated that the EBT was 0.5 s in this condition. The EBT would improve when low power operating devices (materials) were used and/or the circuits were optimized.

5. Conclusion

We proposed a MNV-SRAM using a ReRAM. The proposed 9T3R MNV-SRAM cell can store 2 bits of memory and achieve stable recall against process variations and extended program cycles.

In order to realize the stable recall operation, a certain current (or voltage) is applied to the cell before the power supply is turned on. The voltage of nodes S1 and S2 of cells increases depending on R_{refb} and R_m. When R_{refb} is larger than R_m, $V(\mathrm{S1})$ is lower than $V(\mathrm{S2})$. Therefore, the information stored in R_m can be stably recalled when the power supply for the cell is turned on.

To investigate the stability of recall, we simulated the effect of variations in the width of the transistor of the proposed NV-SRAM cell, the resistance of the sample, and the power supply voltage. For example, when the channel width of the transistor of the cell is narrowed by −20%, the V_{d1} decreases (from −224 mV (0%) to −174 mV (−20%)) at 65 ns. On the other hand, the V_{d2} increases slightly (from 92 mV (0%) to 115 mV (−20%)) at 229 ns. Be that as it may, the recall operation was performed correctly.

In the store operation, the recall operation and the decision operation of whether or not the write pulse is required can be performed simultaneously. The decision operation and circuit are not required when using this proposed scheme.

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