Implementations and learning algorithms of multiple-valued logic networks

氏　　名	曹　其萍
学位の種類	博士（工学）
学位記番号	博乙第289号
学位授与の日付	平成17年9月30日
学位授与の要件	論文博士（学位規則第4条第2項）
学位授与の題目	Implementations and Learning Algorithms of Multiple-Valued Logic Networks （多値論理ネットワークの回路構成及び学習アルゴリズム）
論文審査委員(主査)	木村　春彦（自然科学研究科・教授）
論文審査委員(副査)	村本　健一郎（自然科学研究科・教授），山根　智（自然科学研究科・教授）， 畑上　到（自然科学研究科・教授），南保　英孝（自然科学研究科・講師）

Abstract

Multiple-Valued Logic (MVL) has been the subject of much research over many years. By introducing a pnp current mirrors besides using only the npn current mirrors in multiple-valued I^2L circuit design, this paper proposes a new multiple-valued I^2L circuit with low power, simple structure besides the advantages that all Dao's multiple-valued I^2L circuits have. Furthermore, a fast and dense low-power multiple-valued I^2L circuit that can be made in a standard Schottky process with double-layer metallization is proposed. Propagation delay times below 1ns can be obtained. The multiple-valued I^2L circuits show remarkable functionality and offer significant advantages in terms of high packing density, low power, high speed and reduced LSI circuit complexity compared to the conventional multiple-vakued I^2L circuits.

In this paper, we also propose a multiple-valued logic (MVL) network with functional completeness and develop its learning capability. The MVL network consists of layered arithmetic piecewise linear processors. Since the arithmetic operations of the network are basically a wired-sum and a piecewise linear operation, the MVL network can be trained by the traditional error back-propagation algorithm directly and their implementations should be rather simple and straightforward. Finally, this paper describes a new learning method for Multiple-Value Logic (MVL) networks using the local search method. It is a "non-back-propagation" learning method and appears to be valid for most MVL problems of interest. The learning capability of the MVL networks is confirmed through simulations. The simulation results show very good learning convergence for most performed examples.

Introduction

Multiple-Valued Logic (MVL) has been the subject of much research over many years. The object of this work is to develop new Multiple-Valued Logic (MVL) circuits that can compete with or compare favorably with binary logic circuits and learnable and adaptable multiple-valued logic systems.

In this paper, introducing the pnp current mirrors besides using only the npn current mirrors in multiple-valued I^2L circuit design, we propose a new multiple-valued I^2L circuit with low power, simple structure besides the advantages that all Dao's multiple-valued I^2L circuits have. Circuits to realize multiple-valued MAX, MIN, LIT and SUC functions are designed using both the pnp current mirrors and the npn current mirrors-I^2L current-mode techniques. Direct comparisons of the new multiple-valued I^2L circuits with Dao's multiple-valued I^2L circuits demonstrate significantly less device, smaller power dissipation and higher speed.

Furthermore, a fast and dense low-power multiple-valued I^2L circuit that can be made in a standard Schottky process with double-layer metallization is proposed. The circuit consists of pnp and npn current mirrors, Schottky diodes and a normally operated threshold npn transistor with a merged pnp transistor to clamp the npn transistor and prevent the npn from going too deeply into saturation. Propagation delay times below 1ns can be obtained. The multiple-valued I^2L circuits show remarkable functionality and offer significant advantages in terms of high packing density, low power, high speed and reduced LSI circuit complexity compared to the conventional Multiple-Valued I^2L circuits and the proposed new Multiple-Valued I^2L circuits using both npn and pnp current mirrors, as shown in Table 1.

Table 1 Comparison of the traditional multiple-valued I^2L circuits, the new multiple-valued I^2L circuits using both pnp and npn current mirrors and the fast and dense low-power multiple-valued I^2L circuits using integrated Schottky logic

Circuits	characteristic parameters	traditional multiple-valued I^2L circuit	new multiple-valued I^2L circuit	multiple-valued I^2L circuits using integrated Schottky logic
Maximum gate	average power	2.9	0.9	0.2
	delay	5	5	0.5
	transistors	5	3	2
Minimum gate	average power	3.9	0.9	0.2
	delay	5	5	0.5
	transistors	7	4	2
Successor gate	average power	3.5	1.5	0.3
	delay	5	5	0.5
	transistors	8	7	7
Literal gate	average power	2.9	2.9	0.4
	delay	5	5	0.5
	transistors	8	8	8

In this paper, we also describe a learning MVL network and its algebraic properties, algorithm and applications. We propose a multiple-valued logic (MVL) network with functional completeness and develop its learning capability. The MVL network consists of layered arithmetic piecewise linear processors. Since the arithmetic operations of the network are basically a wired-sum and a piecewise linear operation, their implementations should be rather simple and straightforward. Furthermore, the MVL network can

be trained by the traditional error back-propagation algorithm directly. The learning algorithm that combines back-propagation learning with other features of the MVL networks, including the piecewise linear node function and the multiple-valued representations is presented and appears to be valid for most MVL problems of interest. The algorithm trains the networks using examples and appears to be available for most MVL problems of interest.

This paper describes a new learning method for Multiple-Value Logic (MVL) networks using the local search method. It is a "non-back-propagation" learning method which constructs a layered MVL network based on canonical realization of MVL functions, defines an error measure between the actual output value and teacher's value and updates a randomly selected parameter of the MVL network if and only if the updating results in a decrease of the error measure. The learning capability of the MVL networks is confirmed through simulation. The simulation results show very good learning convergence for most performed examples compared with the traditional back-propagation algorithm, as shown in Fig. 1.

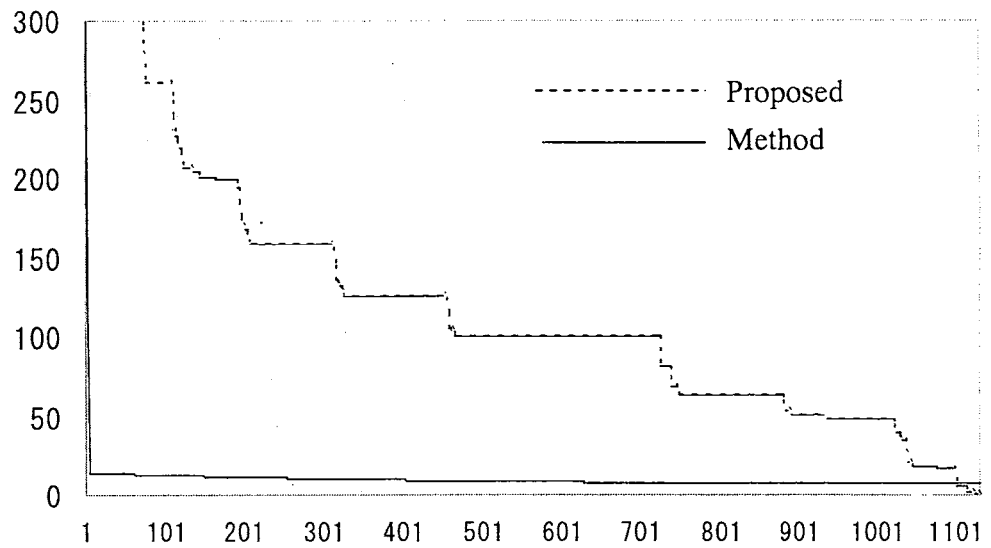

Fig.1 The comparison of convergence performance between the proposed local searching method and the neural network back-propagation method on a 4-variable 4-valued function.

学位論文審査結果の要旨

平成17年7月26日に第1回学位論文審査委員会を開催、8月2日に口頭発表、その後に第2回審査委員会を開催し、慎重審議の結果以下の通り判定した。なお、口頭発表における質疑を最終試験に代えるものとした。

本論文は、画像処理、音声認識、信頼性設計などに応用されている多値論理での新しい回路の提案と、外部環境に適応していく多値論理ネットワークの学習アルゴリズムを提案したものである。まず、高速、高集積度、低消費電力の多値論理回路を提案した。これにより、「素子がいくら小さくても、IC中の配線が80％を占め、更なる高速、高集積度が望めない」という現在の2値論理システムの問題点を打開することができる。次に、誤差逆伝搬学習法を用いた多値論理ネットワークの学習アルゴリズムと、非誤差逆伝搬学習法を用いた多値論理ネットワークの学習アルゴリズムを提案した。前者は単一方向線形関数を持つものであり、多値論理ネットワークが任意の多値論理関数を実現できることを証明した。また、シミュレーションにより優れた学習能力があることを実証した。後者は局所探索法で学習が可能であり、誤差逆伝搬学習法よりも効率が良い。また、アナログ乗算不要のためハードウェアの実現が容易である。

以上の研究成果は、多値論理の研究に大きく貢献するものであり、本論文は博士（工学）に値するものと判定した。