Characterization and Optimization of Avalanche Photodiodes Fabricated by Standard CMOS Process for High-speed Photoreceivers

DISSERTATION ABSTRACT

CHARACTERIZATION AND OPTIMIZATION OF AVALANCHE PHOTODIODES FABRICATED BY STANDARD CMOS PROCESS FOR HIGH-SPEED PHOTORECEIVERS

高速光レシーバの実現に向けたCMOS アバランシェ光検出器の特性評価と最適化

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ABSTRACT

A dissertation presented on the characterization and optimization of avalanche photodiodes fabricated by standard CMOS process (CMOS-APD) for high-speed photoreceivers, beginning with the theory and principle related to photodetector and avalanche photodiodes, followed by characterization, optimization, and wavelength dependence of CMOS-APD, and finally link up with the transimpedance amplifier. nMOS-type and pMOS-type silicon avalanche photodiodes were fabricated by standard 0.18 µm CMOS process, and the current-voltage characteristic and the frequency response of the CMOS-APDs with and without the guard ring structure were measured. CMOS-APDs have features of high avalanche gain below 10 V, wide bandwidth over 5 GHz, and easy integration with electronic circuits. In CMOS-APDs, guard ring structure is introduced for high-speed operation with the role of elimination the slow photo-generated carriers in a deep layer and a substrate. The bandwidth of the CMOS-APD is enhanced with the guard ring structure at a sacrifice of the responsivity. Based on comparison of nMOS-type and pMOS-type APDs, the nMOS-type APD is more suitable for high-speed operation. The bandwidth is enhanced with decreasing the spacing of interdigital electrodes due to decreased carrier transit time and with decreasing the detection area and the PAD size for RF probing due to decreased device capacitance. Thus, an nMOS-type APD with the electrode spacing of 0.84 µm, the detection area of 10 x 10 µm², the PAD size for RF probing of 30 x 30 µm² along with the guard ring structure was fabricated. As a results, the maximum bandwidth of 8.4 GHz at the avalanche gain of about 10 and the gain-bandwidth product of 280 GHz were achieved. Furthermore, the wavelength dependence of the responsivity and the bandwidth of the CMOS-APDs with and without the guard ring structure also revealed. At a wavelength of 520 nm or less, there is no difference in the responsivity and the frequency response because all the illuminated light is absorbed in the p^+-layer and the Nwell due to strong light absorption of Si. On the other hand, a part of the incident light is absorbed in the P-substrate and the photo-generated carriers in the P-substrate are eliminated by the guard ring structure for the wavelength longer than 520 nm, and then bandwidth was remarkably enhanced at the sacrifice of the responsivity. In addition, to achieve high-speed photoreceivers, two types of TIA which are common-source and regulated-cascode TIAs were simulated by utilizing the output of the CMOS-APDs. The figure of merits of gain-bandwidth product was used to find the ideal results of the transimpedance gain and bandwidth performance due to trade-offs between both of them. The common-source TIA produced the transimpedance gain of 22.17 dBΩ, the bandwidth of 21.21 GHz and the gain-bandwidth product of 470.23 THz × dBΩ. Besides that, the simulated results of the regulated-cascode TIA configuration demonstrate 79.45 dBΩ transimpedance gain, 10.64 GHz bandwidth, and 845.35 THz × dBΩ gain-bandwidth product. Both of these TIA results meet the target of this research and further encouraging this successful CMOS-APDs to realize high-speed photoreceivers.

1. INTRODUCTION

Photoreceiver with monolithically integrated photodetectors are attractive and has a good potential of becoming one of the most important communication medium for short-distance optical data transmission for realizing local-area networks (LANs), fiber-to-the-home (FTTH) and board-to-board as well as chip-to-chip high-speed data transmissions. They also can be used in optical storage systems such as Compact Disc Read-Only Memory (CD-ROM), Digital Versatile Disc (DVD) and Blue-ray Disc because it requires optical interfaces. Although high-speed photodetectors are already commercialized mainly been implemented in III-V technology for long-haul optical communication, the technology is expensive. Therefore, it becomes the highest priority that a low-cost system implements in short-distance communication. This has been boost by the invention of low-cost vertical-cavity surface-emitting lasers (VCSELs) as light sources of transmitters. In order to realize the optical interconnection, it is necessary to integrate optical devices such as light sources, optical waveguides, photodetectors with electronic circuits. By using CMOS process, it is possible to easily integrate photodetectors and electronic circuits on same Si substrate with low cost because CMOS process is a mature process.

Furthermore, photodetectors by themselves are generally not sufficient to be integrated with the LSI for optical information processing systems. This is because the output of the photodetector is photocurrent, while the electronic circuit at the subsequent stage is operates with the voltage signal. In most cases, the photocurrent produced by the photodetector is quite weak. Therefore, it is essential to have an electronic circuit along with photodetector that produce the output voltage and has electronic amplification ability before it can be used for further processing. To realize high-speed photoreceiver by using CMOS process which offer state-of-the-art performance, optimization of each device is necessary.

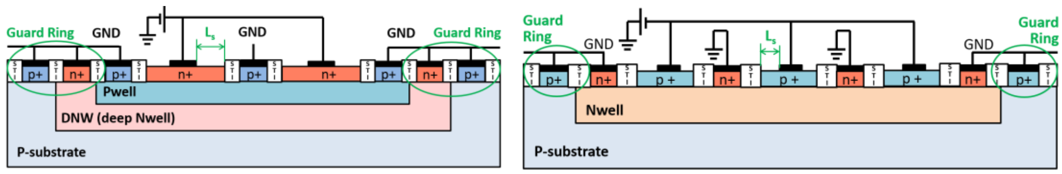
2. OBJECTIVE

The objectives of this research are:

(i) to characterize and optimize the avalanche photodiodes
(ii) to study the wavelength dependence of the avalanche photodiode
(iii) to investigate the transimpedance amplifier that can produce high gain and high bandwidth performance

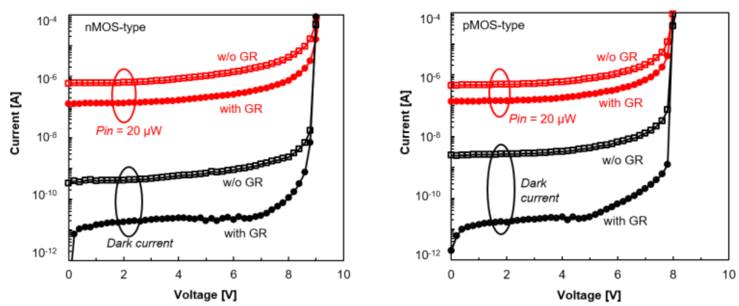
3. CHARACTERIZATION OF CMOS-APD

Figure 1 shows the cross-sectional structure of (a) nMOS-type and (b) pMOS-type CMOS-APDs fabricated by standard 0.18 µm CMOS process without process modifications. The shallow trench isolation (STI) oxides are used as isolation regions between n^+-layer and p^+-layer. The n^+-layer and p^+-layer are arranged alternately and then the electrodes are interdigital structure with the electrode spacing, L_s. The light is illuminated from the top of the device. From the figure, the difference between CMOS-APD with and without the guard ring (GR) structure is found to be the connection of electrodes of the P-substrate and the DNW to the ground in Figure 1 (a), and the connection of electrodes of the P-substrate to the ground in Figure 1 (b). If all electrodes are electrically shorted, it represents the existence of the GR. If not, the structure is without the GR structure, and the P-substrate and the DNW are open for the nMOS-type and the P-substrate is open for the pMOS-type.



(a) nMOS-type CMOS-APD. (b) pMOS-type CMOS-APD.

Figure 1: Cross-sectional structure of fabricated CMOS-APDs.



(a) (b)

Figure 2: Measured I-V characteristics for (a) nMOS-type and (b) pMOS-type CMOS-APDs with and without the GR.

Figure 2 shows the measured Current-Voltage (I-V) characteristics for (a) nMOS-type and (b) pMOS-type CMOS-APDs with and without the GR. The dark current at a low bias is about 10 pA with the GR structure, and the dark current without the GR structure is higher than that with the GR structure. It is because the carriers in the deep layer and the substrate are cancelled due to the GR structure and are not canceled in the CMOS-APD without the GR structure. The breakdown voltage measured when the dark current exceeds 1 μA is about 9.05 V and 8 V for the nMOS-type and pMOS-type, respectively. The breakdown voltage difference for those types may be caused by different doping concentration in the Pwell and the Nwell, which are not disclosed from the manufacturer. Under light illumination at 20 μW, the photocurrent is almost constant for low bias voltage for both types, and it is gradually increased and finally is significantly increased before breakdown voltage due to avalanche amplification.

Figure 3 shows the responsivity of the nMOS-type and the pMOS-type CMOS-APDs with and without the GR as a function of the bias voltage. The responsivity rises initially with the bias voltage because of the increase of the depletion width. It is then dramatically increased at a certain voltage due to avalanche amplification, and the responsivity more than 1 A/W is achieved near the breakdown voltage for all the devices. The responsivity of the CMOS-APDs with the GR is lower than that of without the GR because the quantum efficiency is decreased due to cancellation of photo-generated carriers in the deep layer and the P-substrate.

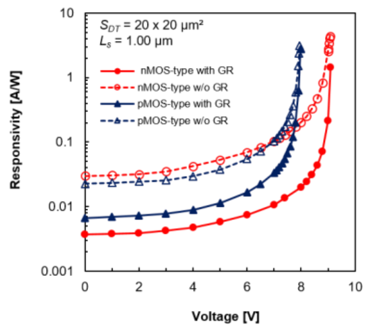
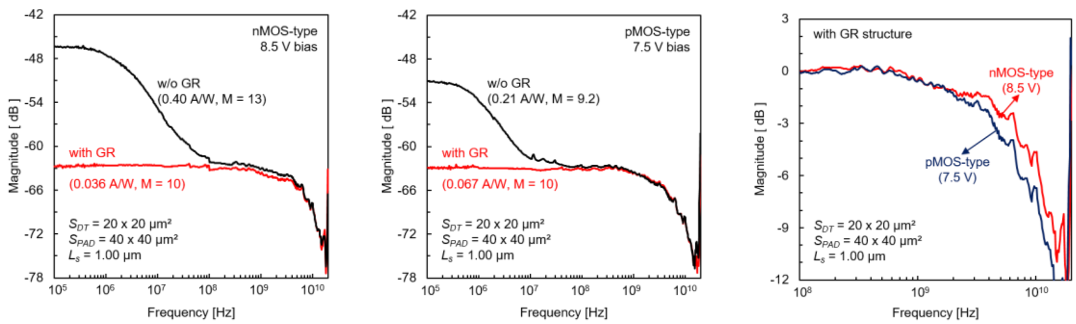


Figure 3: The responsivity of nMOS-type and pMOS-type CMOS-APDs with and without the GR as a function of the bias voltage.



(a) (b) (c)

Figure 4: Frequency response for (a) nMOS-type and (b) pMOS-type CMOS-APD. (c) The comparison of the frequency response between nMOS-type and pMOS-type CMOS-APDs with the GR.

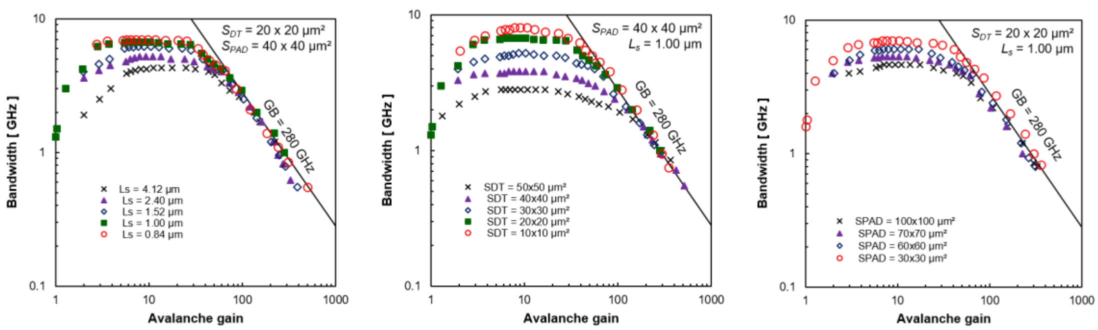
Figure 4 shows the frequency response for (a) nMOS-type and (b) pMOS-type CMOS-APD for 8.5 V and 7.5 V bias voltage, respectively, at 850 nm wavelength. The frequency response for the CMOS-APD with the GR is flat until several GHz. On the other hand, the frequency response of the CMOS-APD without the GR shows high signal magnitude for low frequency region and then dropped to the same signal magnitude with the GR structure around 100 MHz. The large signal magnitude of about 15 dB as compared to the CMOS-APD with the GR at low frequency is due to slow diffusion carriers from the deep layer and the P-substrate. The bandwidth of the CMOS-APD with the GR is three orders of magnitude wider as compared to the CMOS-APD without the GR due to cancellation of photo-generated carriers in the deep layer and the P-substrate which are slow diffusion carriers.

The comparison of the frequency response between nMOS-type and pMOS-type CMOS-APDs with the GR is shown in Figure 4 (c). From the normalized frequency response, the maximum bandwidth for nMOS-type CMOS-APD is 6.77 GHz and is higher than the pMOS-type CMOS-APD of 4.29 GHz. It is due to the quicker avalanche buildup time of electrons compared to the holes, or in other words, the electrons move faster in Pwell rather than holes in Nwell. Therefore, the nMOS-type CMOS-APD with the GR is a suitable candidate for high-speed application.

4. OPTIMIZATION OF CMOS-APD

From previous characterization of nMOS- and pMOS-type CMOS-APD, the nMOS-type CMOS-APD with the GR was selected to be optimize due to higher bandwidth performance. The idea is that the bandwidth can be improved by reducing the carrier transit time due to decreasing the electrode spacing L_s. Bandwidth enhancement also can be achieved by shrinking the detection area and the PAD size for RF probing due to decreased depletion capacitance and the PAD capacitance, respectively. Thus, to incorporate with that idea, the CMOS-APD with several size of the electrode spacing L_s, the detection area S_{DT}, and the PAD size for RF probing S_{PAD} are fabricated.

Figure 5 (a) shows the relation between the avalanche gain and the bandwidth of the CMOS-APDs for different electrode spacing L_s. The detection area S_{DT} and the PAD size S_{PAD} are S_{DT} = 20 x 20 μm^2 and S_{PAD} = 40 x 40 μm^2, respectively. The bandwidth is enhanced with decreasing the electrode spacing is maximized when the avalanche gain is about 10 irrespective of the electrode spacing L_s. The maximum bandwidth of 7 GHz is obtained when the avalanche gain is about 10 for the electrode spacing L_s = 0.84 μm. The gain-bandwidth product is the same irrespective of the electrode spacing L_s and is 280 GHz.



(a) (b) (c)

Figure 5: The relation between the avalanche gain and the bandwidth of the CMOS-APDs for (a) different electrode spacing L_s, (b) different detection area S_{DT}, and (c) different PAD size S_{PAD}.

Figure 5 (b) shows the relation between the avalanche gain and the bandwidth for different detection area S_{DT}. The electrode spacing L_s and the PAD size S_{PAD} are L_s = 1.00 μm and S_{PAD} = 40 x 40 μm^2, respectively. The detection area of 10 x 10 μm^2 shows the largest bandwidth of about 8.0 GHz compared to other sizes. It means that, the smaller detection area enhances the bandwidth, however, too-small detection area causes difficulty of light illumination from top of the CMOS-APD.

Figure 5 (c) shows the relation between the avalanche gain and the bandwidth for different PAD size S_{PAD}. The electrode spacing L_s and the detection area S_{DT} are L_s = 1.00 μm and S_{DT} = 20 x 20 μm^2, respectively. The bandwidth is increased with decreasing the PAD size.

Finally, an nMOS-type CMOS-APD is fabricated with the electrode spacing of 0.84 μm, the detection area of 10 x 10 μm^2 and the PAD size for RF probing of 30 x 30 μm^2 along with the guard ring structure for the purpose of high-speed operation. The relation between the avalanche gain and the bandwidth is shown in Figure 6. The maximum bandwidth of 8.4 GHz, the gain-bandwidth product of 280 GHz, and the responsivity-bandwidth product of 0.7 GHz x A/W are achieved. The maximum bandwidth is achieved at the avalanche gain of about 10 and the responsivity of about 0.02 A/W.

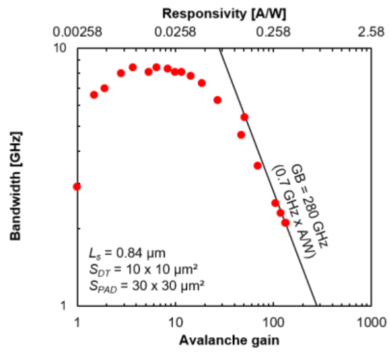


Figure 6: The relation between the avalanche gain, the responsivity and the bandwidth for the optimum nMOS-type CMOS-APD with the guard ring.

5. WAVELENGTH DEPENDENCE

In this section, a pMOS-type CMOS-APD structure was used to investigate the details experimental results on the wavelength dependence of the I-V characteristics, responsivity, and frequency response. It is because the pMOS-type CMOS-APD structure only have Nwell and P-substrate as compared to nMOS-type CMOS-APD, thus, easily to understand the behavior of each wavelength towards avalanche photodiode. The wavelengths of the input optical signal are 400 nm $\leq \lambda \leq$ 850 nm.

Figure 7 shows the measured I-V characteristics for with and without the GR structures at wavelengths of 405 nm, 520 nm, 635 nm and 850 nm. At 405 nm wavelength, the I-V characteristics for both with and without the GR structures are almost the same. This is due to strong optical absorption of Si at 405 nm wavelength, and therefore all the incident light is absorbed in the p^+-layer and the Nwell and does not reach the P-substrate. At 520 nm wavelength, although the photocurrent of the CMOS-APD with the GR is slightly smaller than of the CMOS-APD without the GR, the difference is insignificant. This is because most of the incident light is absorbed in the p^+-layer and the Nwell and only a few reaches the P-substrate region at 520 nm wavelength.

On the other hand, the difference of the I-V characteristics under illumination at 635 nm wavelength was clearly observed for with and without the GR structures, and the photocurrent of the CMOS-APD with the GR is about half as compared to the CMOS-APD without the GR. This is because the optical absorption of Si at 635 nm wavelength is decreased and a small portion of the incident light reaches the P-substrate region. The electrons and holes photo-generated in the P-substrate move toward the n^+-layer and the p^+-

layer, respectively. For the CMOS-APD with the GR, the photo-generated holes are blocked from moving to the Nwell direction by the potential barrier between the Nwell and the P-substrate. As the p^+-layer on P-substrate is connected to the n^+-layer on the Nwell, the photo-generated electrons and holes are recombined and do not contribute to the photocurrent. Only electrons and holes photo-generated in the p^+-layer and the Nwell contribute to the photocurrent, and accordingly the photocurrent is decreased. In contrast, large photocurrent is obtained for the CMOS-APD without the GR because the photo-generated electrons and holes in the P-substrate flow to the electrodes through the low potential barrier between the Nwell and the P-substrate.

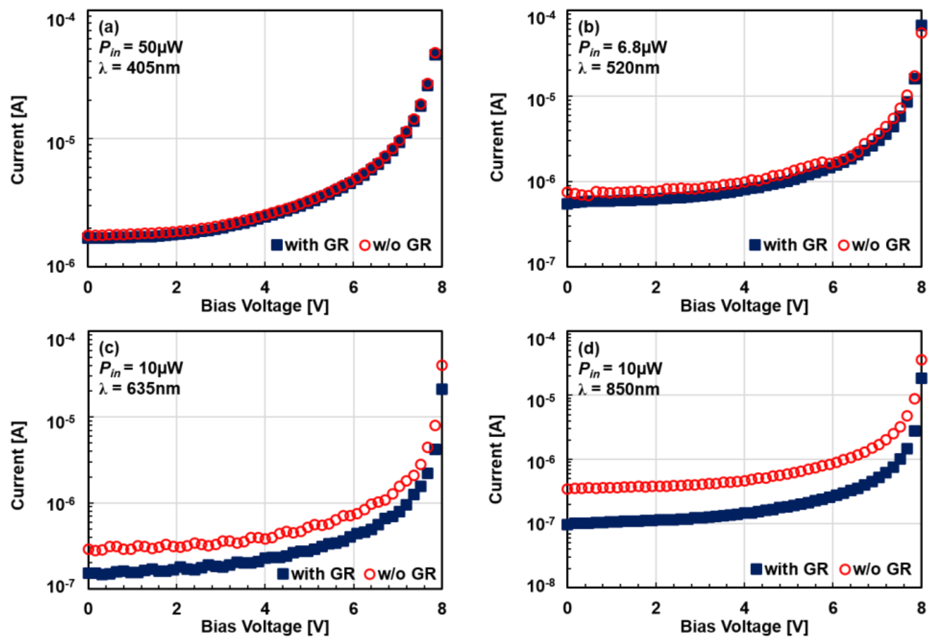


Figure 7: Measured I-V characteristics for different wavelengths.

At 850 nm wavelength, the optical absorption of Si is further decreasing, therefore, more carriers are photo-generated in the P-substrate, and then the magnitude of the photocurrent is hugely affected by the mechanisms of the guard ring described above. For this reason, the difference of photocurrent has spread to around 3.3 times between with and without the GR structures.

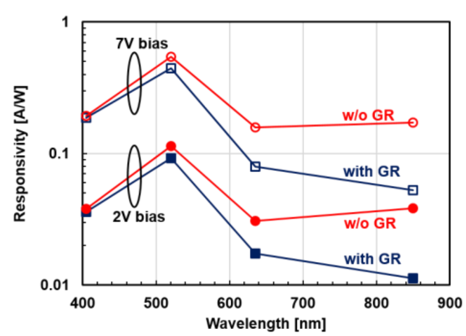


Figure 8: Wavelength dependence of the responsivity.

Figure 8 shows the wavelength dependence of the responsivity at the bias voltage of 2 V and 7 V, obtained from Figure 7. There is no difference in responsivity for both structures at 405 nm wavelength, and the difference increases with increasing the wavelength. At 405 nm wavelength, all the incident light is absorbed in the p^+-layer and the Nwell due to strong optical absorption of Si, and consequently does not reach the P-substrate. As a result, the responsivity is almost same regardless of the guard ring structure. In contrast, due to weak optical absorption of Si at 850 nm wavelength, the incident light can reach the P-substrate region and the GR blocks the photo-generated carriers in the P-substrate, which are slow diffusion carriers, from moving toward the electrodes. Therefore, the reduction of responsivity is more severe with the guard ring. The increased responsivity at 7 V is due to avalanche amplification. The responsivity at 2 V bias (no avalanche gain) for the GR structure at 850 nm wavelength is almost same, and the avalanche gain is also almost similar.

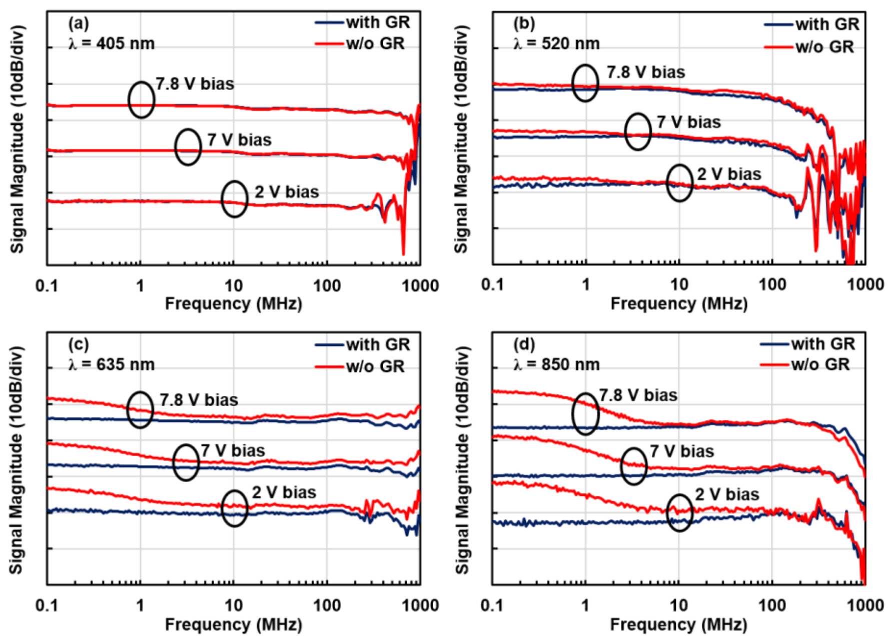


Figure 9: Frequency responses for different wavelengths.

Figure 9 shows the measured frequency response for various wavelengths. At 405 nm wavelength, there is no difference in the frequency response regardless of the guard ring structure because all the incident light is absorbed in the p^+-layer and the Nwell. At 520 nm wavelength, the signal magnitude of the CMOS-APD without the GR is slightly higher than the CMOS-APD with the GR in low frequency region, and no difference in the signal magnitude is observed for frequency range over 10 MHz.

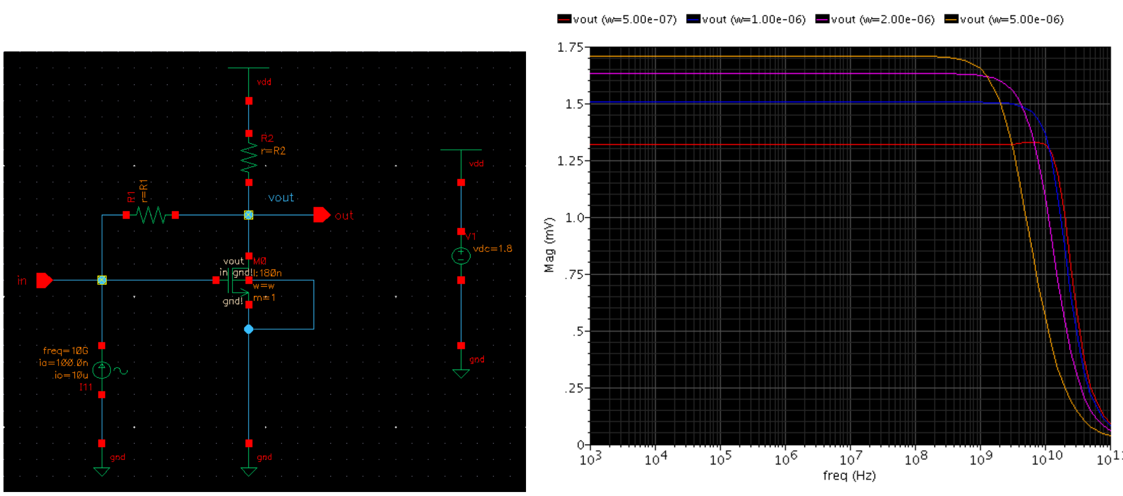
On the other hand, at 635 nm wavelength, the signal magnitude of the CMOS-APD without the GR in low frequency region is obviously higher than the CMOS-APD with the GR. The difference is approximately 6 dB at 100 kHz. This is because the carriers photo-generated in the P-substrate reaches the electrodes and contribute to the photocurrent. As the carriers photo-generated in the P-substrate is slow diffusion carriers due to weak electric field, the signal magnitude is reduced in the frequency of several MHz. At 850 nm wavelength, the difference in signal magnitude in low frequency region becomes more apparent, which is about 10 dB at 100 kHz. There is no difference in the frequency response over 10 MHz regardless of the guard ring structure at 635 nm and 850 nm wavelength. The bandwidth of the CMOS-APD without the GR is about 1 MHz or less, while the bandwidth of the CMOS-APD with the GR is found to be more than 100 MHz, which is limited by the modulation bandwidth of laser sources. The bandwidth of more than 1 GHz is expected for the CMOS-APD with the GR. The bandwidth is significantly improved by the guard ring because slow diffusion carriers photo-generated in the P-substrate are eliminated by the GR structure.

6. TIA

Since the photodiodes produce a small current and the following process attempts in the voltage domain, the current must be converted to voltage. This task can be handle by a transimpedance amplifier TIA, where, the input signal of a TIA is a current and the output signal is a voltage. In this research, there are two TIA design which are common-source and regulated-cascode.

6.1 Common-source TIA

Figure 10 (a) shows the schematic diagram of a common-source (CS) TIA. In this circuit, the gain can be increased or decreased by changing the resistances R1 and R2 or the gate width W of the MOSFET. Although the gain can be increased by increasing the value of each parameter, but, it is different for each parameter. Therefore, it is necessary to select the parameter properly according to the feature. In addition, it is desirable that the gain is large, but as the gain is increased, the range for linear amplification is possibly narrows and maybe the waveform collapses, so it is important to balance with the input signal current.



(a) (b)

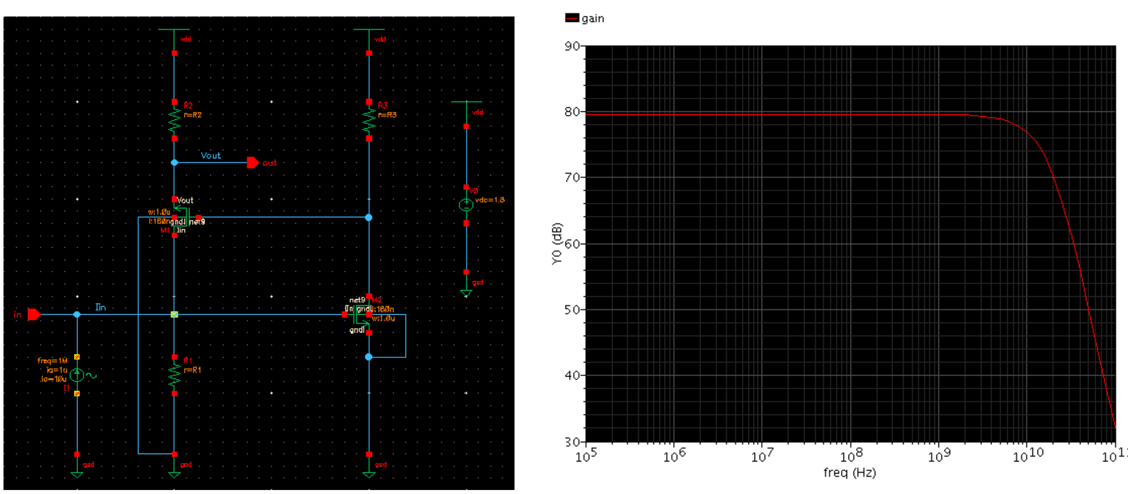
Figure 10: (a) Schematic diagram, and (b) Frequency response of a common-source TIA.

At first, DC analysis of the CS is done by varied the parameters of resistances R1 and R2 and the gate width W. The gate length L of the nMOS is 0.18 µm, which is the minimum value in this technology aims for high-speed response. By using 3 types of R1 and R2: 10 kΩ, 20 kΩ, 50 kΩ, and 5 types of W: 0.5 µm, 1 µm, 2 µm, 5 µm, 36 simulations were performed in total. As a results, the wider the gate width, the steeper the slope of the IV characteristic, therefore, the gain is increased. The gain is also increased if R1 or R2 value increased.

To simulated the frequency response, input of the simulation is AC current and the output voltage is in the logarithmic region, then, a -3 dB bandwidth is obtained. To consider which combination that each parameter gives a wider -3 dB bandwidth, the conditions are similar to DC analysis. A total of 36 simulations were performed by three values of R1 and R2: 10 kΩ, 20 kΩ, 50 kΩ, and four values of W: 0.5 µm, 1 µm, 2 µm, 5 µm. As a results, the resistors that yields the optimum results are R1: 20 kΩ and R2: 50 kΩ. The frequency response for these resistors is shown in Figure 10 (b). As a results, the optimum parameters are R1: 20 kΩ, R2: 50 kΩ, and W: 0.5 µm, that provide the results of transimpedance gain of 22.17 dBΩ, bandwidth of 21.21 GHz and gain-bandwidth product of 470.23 THz × dBΩ.

6.2 Regulated-Cascode TIA

Figure 11 (a) shows the schematic diagram of a regulated-cascode TIA. In this circuit, the photocurrent is amplified to be a voltage at the drain of M1. The M2 and R3 stage are functions as a local feedback to reduce the input impedance by its voltage gain. The input signal used for this circuit is same with previous common-source circuit. The output signal is located between the source of transistor M1 and resistor R2. The input voltage is 1.8 V. The gate length L of all the transistors is 0.18 µm, which is the minimum value in this technology aims for high-speed response.



(a) (b)

Figure 11: (a) Schematic diagram, and (b) Frequency response of a regulated-cascode TIA.

The parameters for this RGC circuit analysis is three types of resistors: R1, R2, and R3. The values are varied for 10 kΩ, 20 kΩ, and 50 kΩ, therefore, a total of 26 simulations were performed. The gate length and width for both transistors are 0.18 µm and 1 µm, respectively. The target bandwidth and transimpedance gain for this RGC TIA are > 9GHz and > 54 dBΩ, respectively. Form all 26 simulations, the optimum combination parameter values of resistors R1, R2, and R3 are 20 kΩ, 10 kΩ, and 10 kΩ, respectively. The bandwidth achieve for this RGC TIA is 10.64 GHz and transimpedance gain of 79.45 dBΩ with the gain-bandwidth product of 845.35 THz × dBΩ. The frequency response is shown in Figure 11 (b).

7. CONCLUSION

The bandwidth of the CMOS-APD is enhanced with the guard ring structure due to elimination the slow photo-generated carriers in a substrate. The bandwidth is also enhanced with decreasing the spacing of interdigital electrodes due to decreased carrier transit time and with decreasing the detection area and the PAD size for RF probing due to decreased device capacitance. Thus, an nMOS-type APD with the electrode spacing of 0.84 µm, the detection area of 10 x 10 µm², the PAD size for RF probing of 30 x 30 µm² along with the guard ring structure was fabricated. As a results, the maximum bandwidth of 8.4 GHz at the avalanche gain of about 10 and the gain-bandwidth product of 280 GHz were achieved. Furthermore, the wavelength dependence of the CMOS-APDs shows that there is no difference in the responsivity and the frequency response at a wavelength of 520 nm or less because all the illuminated light is absorbed in the p^+-layer and the Nwell due to strong light absorption of Si. On the other hand, a part of the incident light is absorbed in the P-substrate and the photo-generated carriers in the P-substrate are eliminated by the guard ring structure for the wavelength longer than 520 nm, and then bandwidth was remarkably enhanced at the sacrifice of the responsivity. In addition, to achieve high-speed photoreceivers, two types of TIA which are common-source and regulated-cascode TIAs were simulated. As a results, the transimpedance gain of 22.17 and 79.45 dBΩ, the bandwidth of 21.21 and 10.64 GHz, and the gain-bandwidth product of 470.23 and 845.35 THz × dBΩ was achieved, respectively.

平成２９年　２月　６日

学位論文審査報告書（甲）

１．学位論文題目（外国語の場合は和訳を付けること。）

Characterization and optimization of avalanche photodiodes fabricated by standard CMOS process for high-speed photoreceivers

（高速光レシーバの実現に向けたCMOSアバランシェ光検出器の特性評価と最適化）

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３．審査結果の要旨（600～650字）

平成29年2月6日に第1回論文審査会を開催し，同日に口頭発表を実施し，その後に第2回審査委員会を開催した。慎重審議の結果，以下のとおり判定した。なお，口頭発表に対する質疑を最終試験に代えるものとした。

本論文は，低コストな光配線に不可欠な集積化高速光レシーバ実現に向けた，CMOSプロセスを用いた高速アバランシェ光検出器（CMOS-APD）に関する研究である。まず，nMOS構造の方がpMOS構造より高速化が可能であること，基板をGNDに接続したガードリング構造が高速化に有利であることを示した。また，受光面積および電極PAD面積を小さくするほど素子容量が小さくなり帯域幅が広がること，電極間隔が狭いほどキャリアの走行距離が短くなり帯域幅が広がることを示し，最終的に最大帯域幅8.4 GHz，利得帯域幅積280 GHzを得た。次に，pMOS構造のCMOS-APDの受光特性の波長依存性について研究を行い，波長405 nmおよび520 nmではガードリングの有無による感度や帯域幅の差異はないが，波長635 nmおよび850 nmではガードリングにより感度は低下するが，帯域幅は広くなることを示した。

以上の研究結果は，CMOSプロセスを用いた光検出器の設計に指針を与え，高速な光配線技術の実現に大きく貢献するものであり，博士（学術）に値すると判断した。

４．審査結果　　(1) 判　　定（いずれかに○印）　合　格　・　不合格

(2) 授与学位　　博　士（　学術　）