A multiplier-less digital timing extractor circuit with round-off error canceller

A MULTIPLIER-LESS DIGITAL TIMING EXTRACTOR CIRCUIT WITH ROUND-OFF ERROR CANCELLER

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ABSTRACT

A simplified digital tuned-circuit timing extractor is proposed. An A/D converter and multipliers are not required. The tuning frequency is determined only by a master clock. The tank circuit output noise is sufficiently suppressed by a newly introduced error canceller. Although a sampling frequency for the tank circuit is relatively low, phase of the output signal is effectively detected. The computer simulation shows phase adjusting for data sampling clock is stable. The proposed timing extractor is easily realized on digital integrated circuits.

I. INTRODUCTION

Many circuits, which are used in digital transmission systems, have been successfuly integrated on LSI circuits. Among them, a timing extractor still needs an analog tank circuit, which is not suited to integrated circuit implementation, or a relatively complicated phase locked loop circuits [1]-[5]. Particularly, when the tank circuit is employed, the tuning frequency is very sensitive to component deviations, and large output noise is caused.

This paper is concerned with a digital tuned-circuit timing extractor. Particularly, stress is placed on digital hardware reduction. For this purpose, an A/D converter and multipliers are eliminated, and a roundoff error canceller is employed. A highly accurate tuned frequency and stable clock phase adjusting are also obtained.

II. DIGITAL TANK CIRCUIT

Pre-processing

A block diagram for a proposed digital tank circuit is shown in Fig. 1. Since the input signal, which is an equalized pulse train, has a continuous time waveform, it must be converted into digital signal. In order to generate timing frequency component, the bipolar coded pulse train is first full wave rectified, and clipped. The clipped waveform is sampled by a frequency of Nf_0, $1 \ll N$, where f_0 is the timing frequency, and its sign is converted into 1 bit digital code. A simple low-pass filter, such as an integrator, is used in order to suppress the high frequency components, which will aliase into the tuned frequency band after sampling rate reduction. Thus, a complicated A/D converter can be eliminated.

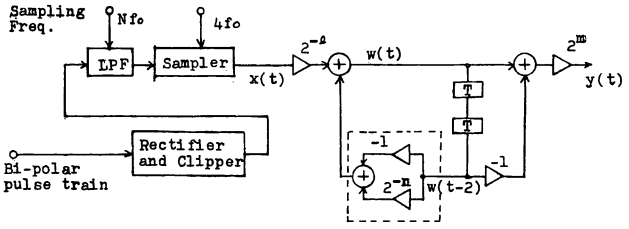

Fig. 1. Digital tank circuit with preprocessing.

Multiplier-less Digital Tank Circuit

The tank circuit is realized with a 2nd-order recursive filter whose transfer function is given by

$$H(z) = h_0 \frac{1 + a_1 z^{-1} + a_2 z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}}, \quad z = e^{j\omega T} \qquad (1)$$

where, $T = 1/f_s$ and f_s is a sampling frequency. The tuning frequency, which must be equal to the timing frequency f_0, is very sensitive to b_1. Therefore, long coefficient wordlenghths, in other words, a complicated multiplier is usually required. By setting f_s to $4f_0$, b_1 becomes exactly zero, and no multiplier is needed. Furthermore, the tuning frequency is completely fixed to f_0.

When b_1 is zero, b_2 determines only Q, which is defined by $f_0/\Delta f$, where Δf is a bandwidth (-3dB). Since Q is not so strictly specified, and in order to eliminate a multiplier for b_2, b_2 is approximated by $1-2^{-n}$. Two single zeros are located at $\omega T = 0$ and π radian, respectively. Consequently, the transfer function becomes

$$H(z) = 2^{-\ell+m} \frac{1 - z^{-2}}{1 + (1 - 2^{-n}) z^{-2}}. \qquad (2)$$

The parameters ℓ, m and n are determined from the following conditions.

(1) $|H(e^{j\omega T})|$ is unity at f_0.
(2) $f_0/\Delta f$ is equal to the specified Q.
(3) L_∞ norm scaling for the first adder output w(t) is employed.

For example, when Q is required to be 100, $n = \ell = 6$ and $m = -1$ result, from the above conditions. The amplitude response for H(z) is illustrated in Fig. 2.

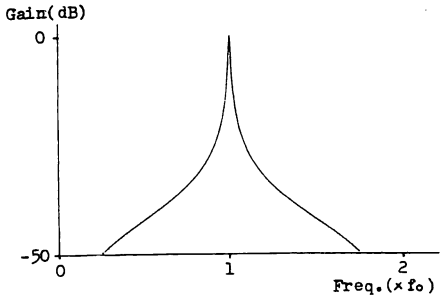

Fig. 2. Amplitude response in dB for digital tank circuit.

III. ROUNDOFF ERROR CANCELLER

In the tank circuit, a noise transfer gain from b_2 to the filter output is 2^n, which is usually very large. In such a case, a long wordlength variable is required in order to meet a specified signal-to-noise ratio. For this reason, a new roundoff error canceller is employed.

Since the roundoff error is caused by the shifter 2^{-n}, the error can be exactly detected before shifting. The shifter output signal, which includes the roundoff error, is returned to the shifter input after passing through two delay elements. Therefore, by returning the detected error to the shifter input after also passing through two delay elements, the error included in the returned signal is completely cancelled.

The above process is illustrated in Fig. 3. Letting $Q[\cdot]$ be a truncation function or a rounding function, equations for the variables indicated in this figure are given by

$$v(t) = w(t-2) + e(t-2) \tag{3}$$

$$w(t) = 2^{-\ell}x(t) - w(t-2) + Q[2^{-n}v(t)] \tag{4}$$

$$e(t) = (Q[2^{-n}v(t)] - 2^{-n}v(t))2^n. \tag{5}$$

When a truncation function is employed for $Q[\cdot]$, a lower significant n bit data becomes e(t). From Eqs. (3)-(5), a transfer function from e(t) to the filter output is given by

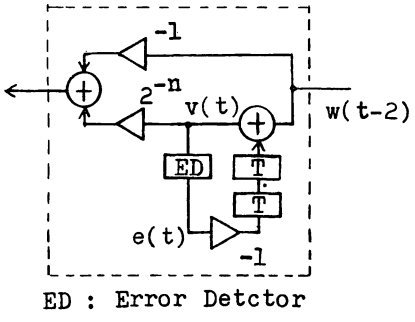

Fig. 3. Roundoff error canceller.

$$H_e(z) = 2^{-n}\frac{1 + z^{-2}}{1 + (1 - 2^{-n})z^{-2}} \tag{6a}$$

$$= 2^{-n}[1 + 2^{-n}z^{-2} - (1 - 2^{-n})2^{-n}z^{-4} \cdots]. \tag{6b}$$

When $2^{-n} \ll 1$, $H_e(z)$ becomes approximately 2^{-n}. On the other hand, letting Δ be the least significant bit, the e(t) values are distributed in the region $(-2^n\Delta/2, 2^n\Delta/2)$. Therefore, the output roundoff noise is expected to be distributed in $(-\Delta/2, \Delta/2)$. This means that the shifter output error is not amplified through being transformed to the filter output. Furthermore, another feature of $H_e(z)$ is to have a zero at f_0 on the unit circle, as shown in Eq. (6a) and Fig. 4. Therefore, a limit cycle of the frequency f_0, which easily occurs in the high-Q tank circuit, is effectively suppressed.

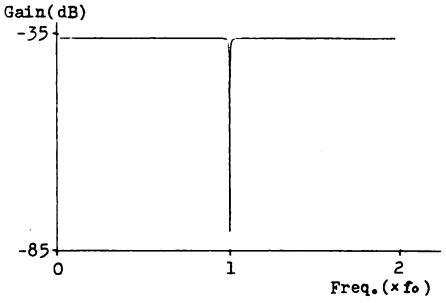

Fig. 4. Amplitude response in dB for $H_e(z)$

Simulation

The tank circuit, whose amplitude response is shown in Fig. 2, is simulated using a periodic input signal with four samples 1, 1, 0, 0 per period, and 16 bit internal variables. The output signal and the output roundoff errors without and with the error canceller are illustrated in Figs. 5(a), (b) and (c), respectively. When the roundoff error is not cancelled, the output error magnitude becomes about $2^n\Delta/2$ in the steady state. On the other hand, by using the proposed error canceller, the output error is sufficiently reduced, and is distributed within $\pm\Delta/2$, as expected previously. Furthermore, since the output error (b) falls into a limit cycle of f_0 in the steady state, it can be effectively suppressed, and is greatly reduced from $\Delta/2$ as shown in Fig. 5(c).

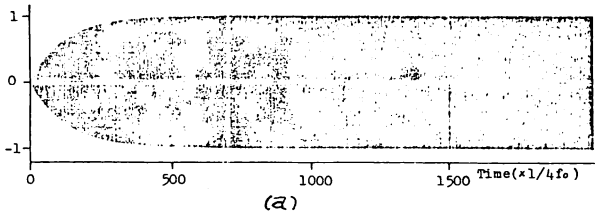

Fig. 5. Simulation of digital tank circuit. (a) Output signal. (b) Output roundoff error without error canceller, and (c) with error canceller.

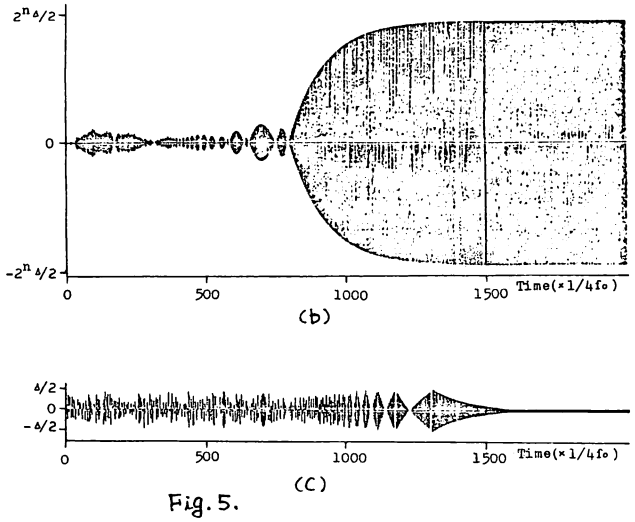

Fig. 5.

IV. PHASE ADJUST FOR DATA SAMPLING CLOCK

Data sampling points are determined from phase information of the tank circuit output. The sampling frequency for the tank circuit is relatively low, that is $4f_0$, as shown in Fig. 6(a). A dotted line indicates the envelope. In order to detect the phase of the envelope directly from the output samples, it is necessary to impose some constraints on the relation between the adjoining samples. Two examples are shown in Figs. 6(b) and (c), in which the samples with symbol * indicate 45 and 0 degrees in phase, respectively. Therefore, by shifting the $4f_0$ clock phase so that the output samples satisfy the above conditions, the output envelope phase can be directly detected from the output sampling point.

Figure 7 shows a block diagram for the proposed phase adjusting method. In the case of Fig. 6(b), when the sample value with the symbol * is larger than that of the succeeding sample, the $4f_0$ clock

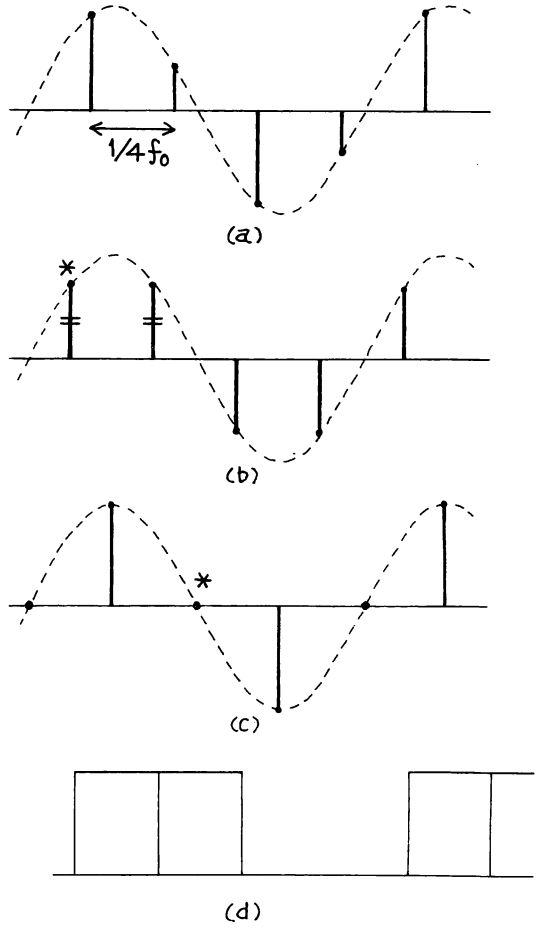

Fig. 6. Digital tank circuit output samples in (a) general case and in (b), (c) specific cases. (d) Clock (f_0) generated from specific sample pattern (b).

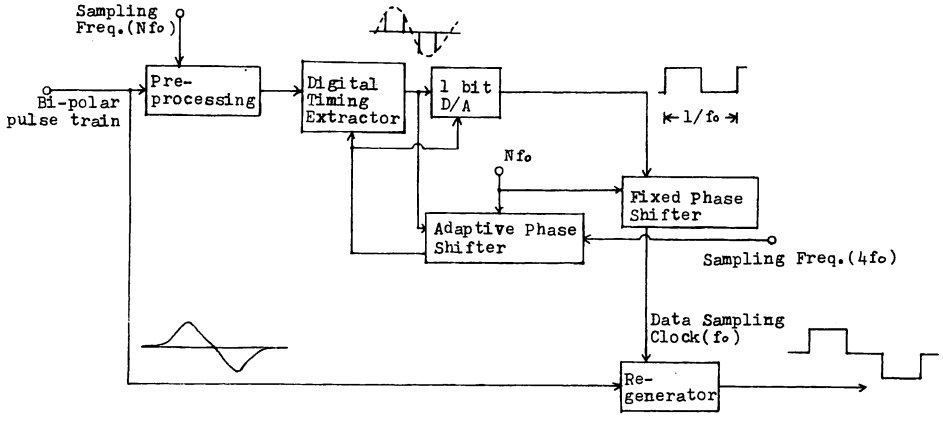

Fig. 7. Phase adjusting for data sampling clock.

phase is shifted to the left side by $1/Nf_0$ sec step, and vice versa. This processing is carried out in an adaptive phase shifter. A data sampling clock (f_0) is obtained from the tank circuit output through a 1 bit D/A converter, as shown in Fig. 6(d). This clock is also shifted by a fixed phase shifter in order to compensate for the delay time from the pre-processing input to the 1 bit D/A converter output.

Simulation

The proposed timing extractor system, shown in Fig. 7, is simulated in a time domain. The parameters n and N are set to 7 and 32, respectively. Q of the tank circuit is 200. The clock phase for the tank circuit is adjusted so that the output samples approach the specified pattern of Fig. 6(b). The phase is shifted by $1/Nf_0$ sec per 128 output samples or 32 data samples. The input signal to the pre-processing is a random data sequence with a mark rate of 1/8. An isolated pulse shaped by a 100 percent roll-off filter is assigned to each data. The resulting clock phase settling behavior is illustrated in Fig. 8. In this figure, "1" and "0" correspond to mark and space, respectively, and the symbol * means the clock phase deviation. The minimum step size is $1/Nf_0$ sec, which is 3 percent of the data sampling period. The clock phase is adjusted after the time response falls into the steady state. In this example, the initial phase deviation is $3x2\pi/N$ radian, and the phase settling time requires 10x32 data samples. The phase deviation in the steady state is within the minimum step size $1/Nf_0$. N and the phase shifting interval are determined from allowable timing jitter and the transient time for the tank circuit, respectively. Furthermore, in order to achieve fast settling as well as stable adjusting for the clock phase, it is desirable to assign different values to the above parameters in the settling interval and the steady state.

V. CONCLUSION

A simplified digital timing extractor has been proposed, which can provide reduced output noise, highly accurate tuned frequency and stable clock phase adjusting. This approach is very suited to digital integrated circuit implementation.

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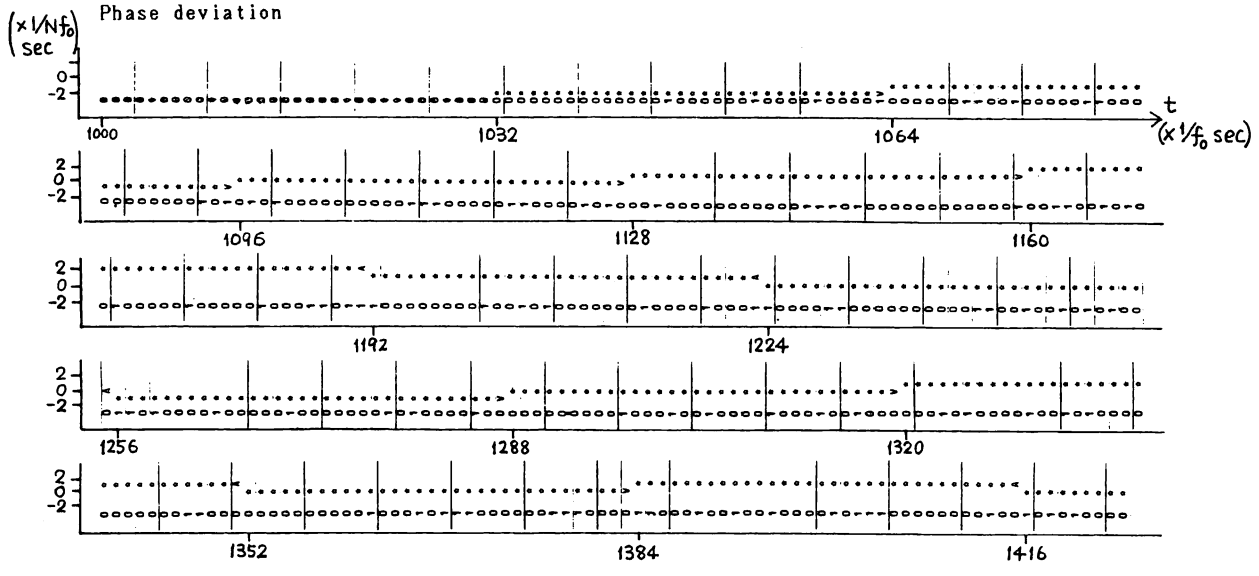

Fig. 8. Simulation for clock phase settling behavior.