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Design Techniques for Switched-Capacitor Adaptive Line Equalizer

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Abstract—This paper describes design techniques for a switched capacitor adaptive line equalizer which is applied to high speed (200 kb/s) digital transmission over analog subscriber loops. An equalizer transfer function is approximated so as to minimize intersymbol interference of an isolated pulse response. Optimum pole–zero location, which is suited to line characteristics in a wide frequency band, is also discussed. In order to attain high accuracy capacitor ratios using a small unit capacitor, capacitor values are rounded off into equivalent integer values, and are discretely optimized using pole–zero deviation as an error criterion. The equalizer has a finite number of frequency responses which correspond to line lengths. Gain and delay time differences between the adjoining step responses are compressed. The designed switched capacitor line equalizer was fabricated using 3-μm CMOS technology. Measured data were very close to designed performances.

I. Introduction

ADVANCEMENT in digital transmission networks and increase in information to be supplied have promoted the development of digital transmission systems utilizing analog subscriber loops [1], [2]. Furthermore, recent LSI technology will make it possible to develop economical and compact digital subscriber transmission systems [3]. Among many technical objectives to be overcome, development of an LSI line equalizer system seems to be most important.

Switched-capacitor (SC) circuits are very suited to realizing the line equalizer on a monolithic MOS circuit with a small chip area and a low power consumption [4]–[7]. One hopeful approach to varying SC circuit characteristics is to discretely change capacitor values using a programmable capacitor array [8]. This kind of variable SC circuit, therefore, has a finite number of step responses. These step responses are individually optimized for the corresponding transmission-line lengths. In order to successfully apply the SC adaptive equalizer to long length transmission lines and high-speed digital transmission, the following technical objectives must be solved. They include transfer function optimization with intersymbol interference as an error criterion, reduction in a total amount of capacitors and compressing gain and delay time differences between the adjoining step responses.

This paper provides design techniques for the SC adaptive line equalizer, which is applied to the time compression multiplexed bidirectional digital transmission over analog subscriber loops [9]. Bit rate is 200 kb/s a line loss at the Nyquist frequency is up to 45 dB. I sions in this paper are mainly directed toward the mentioned objectives.

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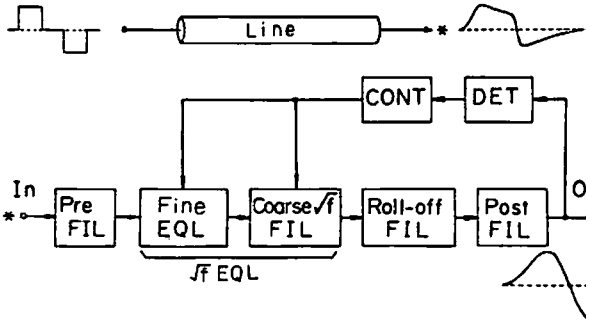

Fig. 1. Adaptive line equalizer system.

Section II briefly describes a functional block di for a line equalizer system. In Section III, an appr tion algorithm for an equalizer transfer function i vided. Reductions in the gain and delay time diffe are discussed in Section IV. Section V describes configurations for SC equalizers. A discrete optimi algorithm for capacitor values is provided in Sectic Finally, Section VII presents examples for designe equalizer characteristics and fabricated LSI perform

II. System Description

Fig. 1 shows a functional block diagram for an ad line equalizer system. Bipolar coded digital signals ha 50-percent duty rectangular pulse are transmitted th the analog subscriber loops. The transmitted pulse is g distorted by the line characteristics. In other words, intersymbol interference (ISI) results, and error rate q in terms of a signal-to-noise ratio is highly deg Before detecting the received pulse, it is optimally s through the line equalizer system. Generally speakin line characteristics are equalized by a $\sqrt{f}$ equalizer (and it's output waveform is shaped so as to minimi through a roll-off filter.

The $\sqrt{f}$ EQL and the roll-off filter are realized wi circuits. Therefore, a pre-filter and a post-filter are ut for anti-aliasing and smoothing waveforms, respect The $\sqrt{f}$ EQL consists of a coarse $\sqrt{f}$ EQL and a fine The line characteristics are mainly equalized by the c $\sqrt{f}$ EQL. The fine EQL, which has approximate fla

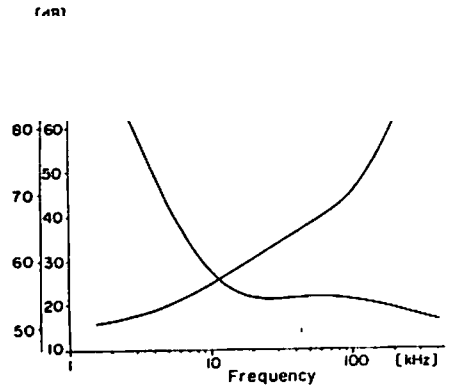

Fig. 2. Frequency responses for 0.5-mm Ø line with 5.9-km length (45-dB loss at 100 kHz).

plitude responses, is used for further adjusting gain differences between the adjoining step responses of the coarse $\sqrt{f}$ EQL. The $\sqrt{f}$ EQL gain is automatically controlled so that the post-filter output level approaches the reference level.

III. Coarse $\sqrt{f}$ EQL Transfer Function Approximation

A. Sampling Frequency

In order to realize high-frequency SC equalizer circuits with a low power consumption, as well as a small chip area, a total amount of capacitances must be well reduced. On the other hand, the capacitor ratio range is proportional to both a sampling frequency and equalizer gain. Therefore, it is desirable to reduce a sampling frequency and to divide a total gain into the equalizer and other blocks. In such a case, however, circuit complexity for both analog pre- and post-filters may be increased. Specifications for these filters are determined from anti-aliazaing the 50-percent duty pulse spectrum and channel noises, and smoothing the SC filter output waveform so as to precisely detect the top or bottom and zero cross points. An useful approach to simplify these analog filters is to employ a low-order SC low-pass filter with a higher clock rate than that for the equalizer [10]. For example, the pre-filter can be constructed as a combined form of a second-order active RC filter and a second-order SC filter. The post-filter is also simplified by operating the roll-off filter with a high sampling frequency.

For these reasons, the sampling frequency for the equalizer is chosen to be relatively low, that is four times as high as data bit rate.

B. Pole–Zero Location

An example of the transmission line characteristics is shown in Fig. 2. Next, pole–zero locations, which are adopted for equalizing these amplitude and group delay responses, are illustrated in Fig. 3. A major part of the equalizer response is formed with Z_1. The characteristics in the low- and middle-frequency bands are further compensated for by using Z_2 and P_1. The reason Z_2 is located

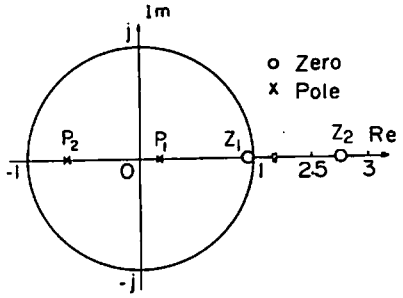

Fig. 3. Pole–zero locations for coarse $\sqrt{f}$ EQL transfer fi

outside the unit circle is explained as, the transmi group delay distortions being somewhat smaller group delay distortions in the minimum phase P_2 located on the negative real axis is used to forr amplitude response in the high-frequency band.

The pole–zero location illustrated in Fig. 3 i equalize the line characteristics shown in Fig. 2. U of this pole–zero location for arbitrary line lengt firmed through the actual design process. For type of lines and frequency bands, optimum locations must be further discussed based on th between line amplitude and group delay response

C. Approximation Algorithm

Data transmission quality is directly evaluat error rate in terms of a signal-to-noise ratio. I equivalently estimated by intersymbol interferenc an isolated pulse response. The proposed algorith fore, approximates a transfer function by using and zeros, given in Fig. 3, as variables and ISI as an error criterion.

Let $g(t)$ be an isolated pulse response for the whole system shown in Fig. 1, which does not, however, include the coarse $\sqrt{f}$ EQL. The other filters are de in advance, and are fixed in the time domain appro ion. Furthermore, an impulse response for the coarse QL is denoted by $h(t)$. Then an isolated pulse respor the whole system can be expressed as

$$f(t) = \int_0^t h(\tau) g(t-\tau)\, d\tau. \tag{1}$$

Letting T_0 be a sampling point at which $f(t$ the maximum value, the received pulses are samp t_n given by

$$t_n = T_0 + nT, \qquad n = \text{integer}\ (\neq 0) \tag{2a}$$

$$T = 1/f_0, \qquad f_0\text{: data rate.} \tag{2b}$$

ISI is usually evaluated by an absolute sum of or a root mean square of $f(t_n)$. The absolute sum (t_n) estimates the worst case, and closely relates to pen- ings. Hence, it is employed as an error criteri d is expressed by

$$E = \sum_{\substack{n=n_1 \\ \neq 0}}^{n_2} w(n) |f(t_n)/f(T_0)| \tag{3}$$

where $w(n)$ is a weighting coefficient.

The proposed algorithm minimizes E through an iterative method, which locally employs a linear programming technique. In the following discussions, the poles and zeros are denoted by

$$\begin{aligned} x_1 &= Z_1 \\ x_2 &= Z_2 \\ x_3 &= P_1 \\ x_4 &= P_2. \end{aligned} \tag{4}$$

Let a vector consisting of x_i be x, and x at the rth iteration step be expressed as $x^{(r)}$. The isolated pulse response $f(t)$ using $x^{(r)}$ is denoted by $f(x^{(r)}, t)$. When deviations in $x^{(r)}$ are assumed to be sufficiently small, $\Delta x^{(r)} \ll 1$, $f(x^{(r)} + \Delta x^{(r)}, t_n)$ is approximately expressed as

$$f\left(x^{(r)} + \Delta x^{(r)}, t_n\right) \approx f\left(x^{(r)}, t_n\right) + \sum_{i=1}^{K} \Delta x_i^{(r)} \left(\frac{\partial f(x, t_n)}{\partial x_i} \right)_{x = x^{(r)}}. \tag{5}$$

If $x^{(r)}$ is assumed to be constant, $f(x^{(r)}, t_n)$ and $(\partial f(x, t_n)/\partial x_i)_{x=x^{(r)}}$ also become constant and, consequently, (5) can be regarded as a linear combination of $\Delta x_i^{(r)}$. Equation (5) is rewritten as

$$f\left(x^{(r)} + \Delta x^{(r)}, t_n\right) = A_n^{(r)} + \sum_{i=1}^{K} B_{n,i}^{(r)} \Delta x_i^{(r)} \tag{6}$$

where

$$A_n^{(r)} = f\left(x^{(r)}, t_n\right) \tag{7a}$$

$$B_{n,i}^{(r)} = \left(\frac{\partial f(x, t_n)}{\partial x_i} \right)_{x = x^{(r)}}. \tag{7b}$$

Next, the absolute sum of $f(x^{(r)}, t_n)$, given by (3), is expressed as a linear combination of $f(x^{(r)}, t_n)$ by using sign coefficients $\delta(n)$ expressing the polarility of $f(x^{(r)}, t_n)$ as follows:

$$E^{(r)} = \sum_{\substack{n=n_1 \\ \neq 0}}^{n_2} \delta(n) w(n) f\left(x^{(r)}, t_n\right) \tag{8a}$$

$$\delta(n) = \begin{cases} 1, & 0 \leqslant f\left(x^{(r)}, t_n\right) \\ -1, & f\left(x^{(r)}, t_n\right) < 0 \end{cases} \tag{8b}$$

where $|f(x^{(r)}, T_0)|$ is normalized as unity. From (6) and (8), minimizing E can be formulated as follows:

$$0 \leqslant \delta(n) \left(A_n^{(r)} + \sum_{i=1}^{K} B_{n,i}^{(r)} \Delta x_i \right) \tag{9a}$$

$$\tilde{E}^{(r)} = \sum_{\substack{n=n_1 \\ \neq 0}}^{n_2} \delta(n) w(n) \left(A_n^{(r)} + \sum_{i=1}^{K} B_{n,i}^{(r)} \Delta x_i \right) \tag{9b}$$

$$\tilde{E}^{(r)} \rightarrow \text{Minimized.} \tag{9c}$$

Since (9) is expressed as a linear equation in $\Delta x_i^{(r)}$, this problem can be reduced to the linear programming. In (9), solved for all possible combinations of $\delta(n)$. In applications, however, useful combinations can be to some extent.

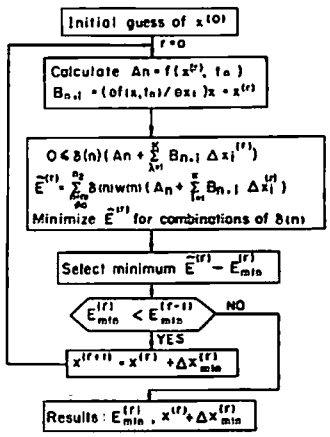

Fig. 4. Approximation algorithm for coarse $\sqrt{f}$ EQL transfer

Among the solutions, the minimum $\tilde{E}^{(r)}$ and th sponding variable $\Delta x^{(r)}$ are chosen. They are den $E_{\min}^{(r)}$ and $\Delta x_{\min}^{(r)}$, respectively. The initial values, $(r+1)$th iteration step, are given by

$$x^{(r+1)} = x^{(r)} + \Delta x_{\min}^{(r)}.$$

At the $(r+1)$th step, the same procedure is repea the iteration step, where $E_{\min}^{(r+1)} < E_{\min}^{(r)}$ is not h approximation is completed. A general flow chart s the proposed algorithm is given in Fig. 4.

Frequency Response:

After the time domain approximation, the gain Nyquist frequency ($f_N = f_0/2$) is adjusted to the s level. Actual gain levels for the coarse $\sqrt{f}$ EQL are down in order to compress the capacitor ratio ran shifted gain level is compensated for by other bloc

Monotonic Capacitor Values:

When variable capacitor values monotonically or decrease in ascending order of the equalizer gain control circuit becomes very simple. For this purp poles and zeros are constrained so as to monot increase or decrease, according to the equalizer ga in the approximation process.

IV. Design of Fine Equalizer

A. Gain Adjust

Fig. 5 shows two approaches A and B to combin responses of the coarse $\sqrt{f}$ EQL and fine EQL. step numbers for the coarse $\sqrt{f}$ EQL and fine E and j, respectively, a combined step is denoted b Furthermore, the zeroth and $(N-1)$th steps corres the minimum and maximum gain levels, respectiv amplitude responses at the $(m-1, N-1)$th and steps become short and over equalizations, in the $\sqrt{f}$ characteristic, respectively. Effects of these de on the isolated pulse response were investigated computer simulation. The results show the short e

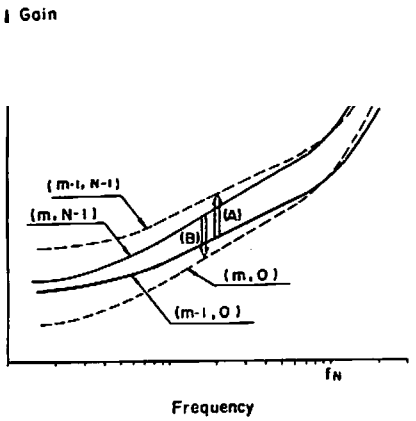

Fig. 5. Two approaches to combining coarse $\sqrt{f}$ EQL and fine EQL step responses.

ing many data sampling points. On the other hand, negative deviation, caused by the over equalization, is mainly concentrated within two time slots. This deviation is effectively cancelled by a decision feedback equalizer with a few taps [7]. Therefore, the approach B is employed.

In the coarse $\sqrt{f}$ EQL transfer function approximation, the fine EQL is fixed to the $(N-1)$th step.

B. Delay Time Adjust

Another problem of the step variable equalizer is delay time difference. The delay time differences between the adjoining step responses of the coarse $\sqrt{f}$ EQL result in timing jitter and degrade error rate quality. The fine EQL purposes include compensation for this difference. The adjoining combination steps, where the coarse $\sqrt{f}$ EQL step response is changed, are expressed as $(m-1, N-1) \rightleftarrows (m,0)$. Letting $\Delta T_{m-1,m}$ be the delay time difference between the $(m-1)$th and mth coarse $\sqrt{f}$ EQL steps, it can be completely compensated for by designing the fine EQL so that the delay time difference $\Delta t_{N-1,0}$ between the $(N-1)$th and 0th steps satisfies

$$\Delta T_{m-1,m} + \Delta t_{N-1,0} = 0. \tag{11}$$

In actuality, however, $\Delta T_{m-1,m}$ slightly differs from step to step. Therefore, the mean value for $\Delta T_{m-1,m}$, $1 \leqslant m \leqslant N-1$, is reduced to zero. Furthermore, delay times for the intermediate steps of the fine EQL are determined so as to gradually vary.

The fine EQL is designed using a first-order transfer function having only one pole.

V. Circuit Configurations

A. Coarse $\sqrt{f}$ Equalizer

The transfer function with the poles and zeros given in Fig. 3 can be synthesized by using the E circuit among a family of active SC biquads [12]. The circuit configuration and its transfer functions are given in Fig. 6 and by (12), respectively.

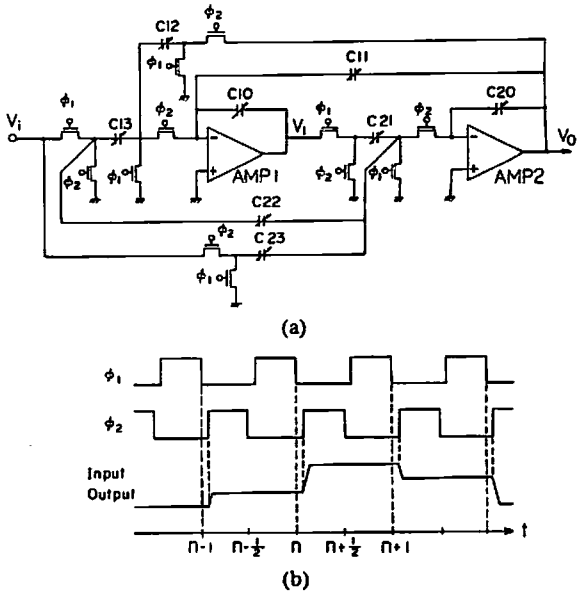

Fig. 6. (a) Circuit configuration for coarse $\sqrt{f}$ EQL. (b) Clo and sampling points.

$$\frac{V_0}{V_i} = -\frac{C_{23} - (C_{23}+C_{22})z^{-1} + (C_{22} - C_{21}C_{13})z^{-2}}{1 + (C_{21}C_{12} + C_{21}C_{11} - 2)z^{-1} + (1 - C_{21}C_{11})z^{-2}}$$

$$C_{10} = C_{20} = 1.$$

Variable capacitors are constructed as a progra capacitor array, as shown in Fig. 7. Appropriate capacitors are selected through switches to realize able capacitor in a parallel form. Since the variable tor values are designed so as to vary in ascen descending orders, according to increasing the e gain level, the differences between the adjoini capacitors are prepaired as the branch capacitors. control signals also become very simple in this way.

This kind of variable SC equalizer usually cause sirable responses, such as spike and transient resp the instant of discretely changing the capacitor val object of the present study, however, is limited to compression multiplexed bidirectional transmiss mentioned previously. Therefore, the above respo be prevented by changing the capacitors during a t ting mode in which the $\sqrt{f}$ EQL is not used.

B. Fine Equalizer

Fig. 8 shows the circuit configuration for the fi with one pole. The transfer function is expressed by

$$\frac{V_0}{V_i} = \frac{C_{12}z^{-1}}{C_{11} + C_{10}(1 - z^{-1})}.$$

Gains at the Nyquist frequency and delay time trolled by C_{12} and C_{10}, respectively.

$$\frac{V_1}{V_i} = -\frac{(C_{23}C_{12} + C_{23}C_{11}) + (C_{13} - C_{22}C_{12} - C_{22}C_{11} - C_{23}C_{11})z^{-1} + (C_{11}C_{22} - C_{13})z^{-2}}{1 + (C_{21}C_{12} + C_{21}C_{11} - 2)z^{-1} + (1 - C_{21}C_{11})z^{-2}}$$

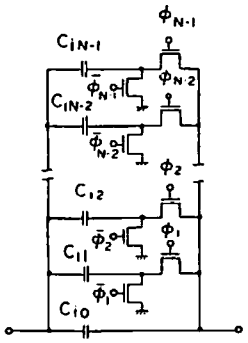

Fig. 7. Variable capacitor array.

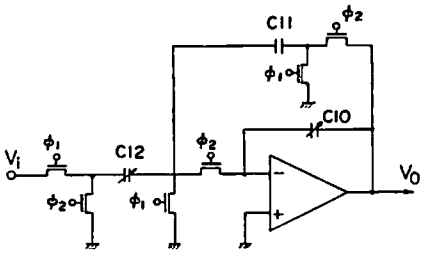

Fig. 8. Circuit configuration for fine EQL.

VI. Discrete Optimization of Capacitor Values

A. Integer Value Capacitors

In order to achieve high accuracy capacitor ratios using small capacitors on monolithic MOS circuits, it is desirable to realize arbitrary capacitors with a plural number of the same dimensional unit capacitors. In this case, capacitor values are equivalently represented to integer values. The integer value capacitors also make it possible to simplify the programmable capacitor array and the control signals.

B. Discrete Optimization Algorithm

Positive real capacitors, obtained from (12) and through scaling the operational amplifier outputs, are rounded off into discrete values. The roundoff error effects on the SC equalizer response have to be minimized [13].

Since discretely searching for optimum capacitors usually requires a large number of computations, the pole and zero deviations are employed as an error criterion instead of ISI.

Let the poles and zeros obtained through the time domain approximation in Section III and rounding off capacitor values be x_i and x_{Ri}, respectively. The distance between x_i and x_{Ri}, which is defined by

$$D = \sum_{i=1}^{K} w_i |x_i - x_{Ri}| \tag{14a}$$

$$w_i = \frac{1}{|1 - x_i|}, \qquad 0 \leqslant x_i \tag{14b}$$

$$= \frac{1}{|1 + x_i|}, \qquad x_i < 0 \tag{14c}$$

is employed as an error criterion. A weighting coefficient w_i

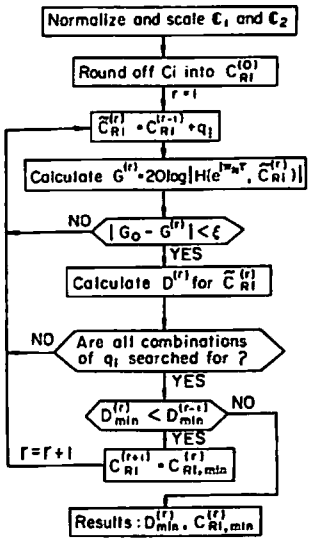

Fig. 9. Discrete value capacitor optimization algorithm.

The capacitors in the SC biquad shown in Fig. 6 divided into two groups,

$$\mathbb{C}_1 = (C_{10}, C_{11}, C_{12}, C_{13})$$

$$\mathbb{C}_2 = (C_{20}, C_{21}, C_{22}, C_{23}).$$

Since the SC circuit performances valid for $\mathbb{C}_1$ an multiplied by constants, they are first scaled by propriate constants R_1 and R_2, and are rounded off integer values. These scaling factors are determined b lower bound for integrator capacitors and the rour error effects, and the upper bound for a total amou capacitances.

Let the initially rounded off capacitor values be $C_R^{(}$ the 1st step, the optimum capacitances are discr searched for around $C_{Ri}^{(0)}$.

Letting

$$\tilde{C}_{Ri}^{(1)} = C_{Ri}^{(0)} + q_i$$

where, q_i is an integer in the restricted region, the criterion D given by (14) is calculated for all po combinations of $\tilde{C}_{Ri}^{(1)}$. Among the above $D^{(1)}$, the mini $D^{(1)}$ and the corresponding $\tilde{C}_{Ri}^{(1)}$ are selected. The denoted as $D_{\min}^{(1)}$ and $C_{Ri,\min}^{(1)}$, respectively. $C_{Ri,\min}^{(1)}$ is us the initial capacitance at the 2nd step, as expressed by and the same searching procedure is repeated.

$$\tilde{C}_{Ri}^{(2)} = \tilde{C}_{Ri,\min}^{(1)} + q_i.$$

At the step where $D_{\min}^{(r+1)} < D_{\min}^{(r)}$ is not held, the di optimization is completed.

Tolerance is imposed on the equalizer gain at the Ny frequency. The capacitor combinations, with whic gains meet the given tolerance, are only adopted for fu evaluation of D.

The algorithm described above is shown as a flow in Fig. 9.

VII. Design Examples

The line equalizer system was designed for 200

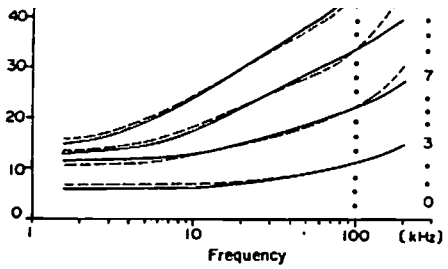

Fig. 10. Amplitude responses in decibels for coarse $\sqrt{f}$ EQL.

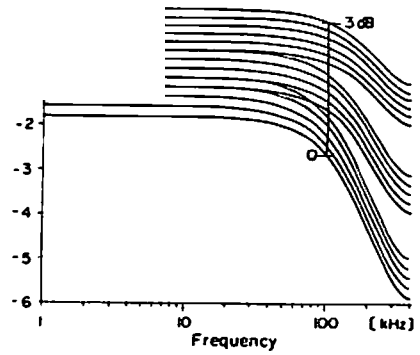

Fig. 11. Amplitude responses in decibels for fine EQL.

loss at 100 kHz. Sixteen kinds of step responses are assigned to both the coarse $\sqrt{f}$ EQL and the fine EQL. Hence, 256 step responses can be realized as a whole, and gain difference becomes about 0.2 dB ($\approx$ 45 dB/256 steps).

A. Coarse $\sqrt{f}$ EQL

Transfer Function Approximation:

In the time-domain approximation, ISI is evaluated in the interval from T_0-2T to T_0+5T, that is $n_1=-2$ and $n_2=+5$, and $w(n)$ values are chosen to be unity for all sampling points. The resulting ISI is less than 9 percent for all step responses. Examples of amplitude responses in decibels are shown in Fig. 10.

Discrete Optimization:

The capacitor values were discretely optimized using the scaling factors, $R_1=4$ and $R_2=8$[1] in the region of $C_{R_i}^{(r)}+q_i$, $-3\leqslant q_i\leqslant+3$, which has seven grids for each capacitor. The tolerance for the gain deviation at 100 kHz is 0.3 dB. In the 15th step response, for instance, a gain of 15.07 dB (target: 14.90 dB, which is shifted down by 30.1 dB) and pole–zero deviation of 9.1 percent after only rounding off are improved to 14.94 dB and 2.7 percent, respectively. Degradations on the eye openings after optimization are very small.

Capacitor Ratio Range:

The coarse $\sqrt{f}$ EQL gain levels for three groups of step responses, that is 0–5th, 6–10th, and 11–15th steps, are shifted by -6.0, -18.1, and -30.1 dB, respectively. As a result of the 800 kHz sampling frequency and the above gain level shift, the capacitor ratio ranges[2] for C_1 and C_2 are reduced to 27.8 and 12.6, respectively, over all steps.

B. Fine EQL

Three kinds of group delay responses were designed for the fine EQL. At the same time, the gain at 100 kHz is equally divided by about 0.2 dB steps. The amplitude responses are shown in Fig. 11. Delay time differences between the adjoining coarse $\sqrt{f}$ EQL step responses are

[1] Capacitor values before scaling, are normalized so that the minimum value is unity.

[2] The capacitor ratio range means a ratio of the maximum and minimum capacitances in this paper.

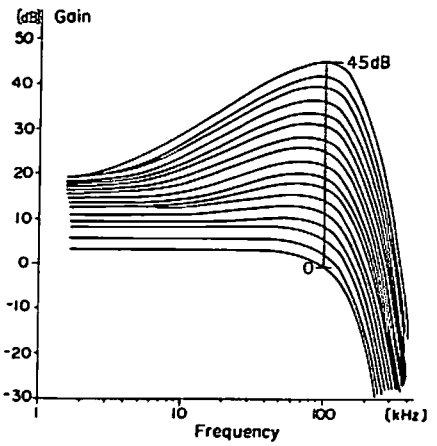

Fig. 12. Amplitude responses in decibels for line equali

up to 0.34 μs, which is 6.8 percent of a dat
period 5 μs ($=1/200$ kHz), and is not negl
delay time difference is compressed to 0.14 μs (

C. Line Equalizer System

The pre-filter is synthesized by combining a s
RC active filter and a second-order SCF wi
sampling frequency than 800 kHz. The cutof
(-3 dB) was determined to be 300 kHz, taking
errors into account. The post-filter is a thir
active filter having a 270-kHz cutoff frequency.
filter is realized with a fourth-order SCF ha
proximate 100-percent roll-off cosine amplitud
Amplitude responses for the line equalizer syst
ing the filters and the $\sqrt{f}$ EQL, are given
Furthermore, frequency responses for a whole
ther including a 50-percent duty rectangular pu
transmission line with the maximum length, i
Fig. 13. This figure shows that an approximate
cosine roll-off response is obtained for a whole
14 shows a calculated eye opening correspon
frequency responses in Fig. 13. When an eye o
is measured by a ratio of the inside and outsid
for the eye opening, the rates for all step res
greater than 80 percent.

Suzuki *et al.* [6] reported a simplified equal
effectively combining a second-order $\sqrt{f}$ EQL

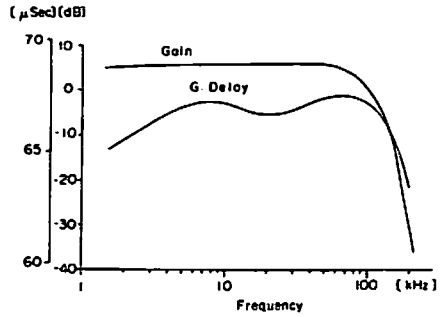

Fig. 13. Amplitude and group delay responses for a whole system including pulse waveform, 0.5-mmØ line with 5.9-km length and line equalizer system having the maximum gain level 45 dB at 100 kHz.

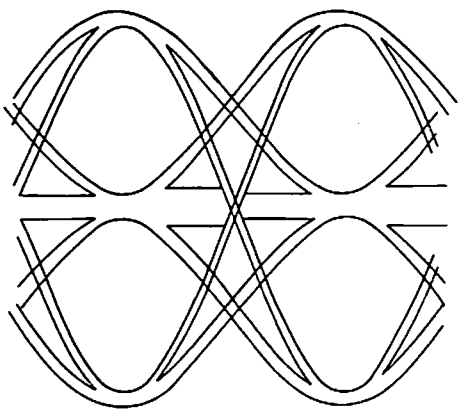

Fig. 14. Calculated eye pattern corresponding to the frequency responses shown in Fig. 13.

order roll-off filter. Since data is detected at the SC equalizer output, the clock phase should be synchronized to the bit rate (200 kHz) so that the top or bottom of the waveform is just sampled [14]. On the other hand, in our approach, the SC circuits operate with asychronous clock phase, and the sampled and held waveform must be well smoothed before data detection. In addition to this, a high gain SC equalizer system is expected to induce relatively large various kinds of noises. For these reasons, higher stopband attenuation is assigned to the roll-off filter compared with the above approach [6]. Furthermore, in order to simplify programmable capacitor arrays and control circuits, the roll-off filter response is fixed.

D. LSI Implementation

The designed line equalizer system was fabricated using 3-μm CMOS technology [15]. The measured data are very close to the designed performances. An example of the measured eye opening for a 5.9-km long 0.5-mmØ transmission line is shown in Fig. 15.

IX. Conclusion

Design techniques for a SC adaptive line equalizer have been proposed. Particularly, this paper has placed stress on the following subjects. They include optimum pole–zero location, transfer function approximation in a time do-

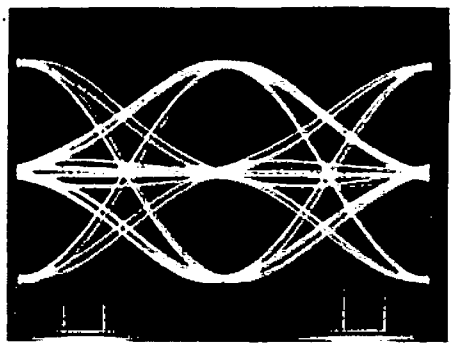

Fig. 15. Measured eye pattern for 0.5-mmØ line with 5.9 km l

time differences. The line equalizer system, which plied to 200 kb/s digital transmission over the 0.5- line, was designed through the proposed metho desirable performances were obtained. An LSI was cated using 3-μm CMOS technology. The measure were very close to the calculated performances.

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