An adaptive SC line equalizer system for four-wire full-duplex and multirate digital transmission

An Adaptive SC Line Equalizer System for Four-Wire Full-Duplex and Multirate Digital Transmission

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Abstract —This paper describes an adaptive switched-capacitor (SC) line equalizer system, which can be applied to four-wire full-duplex and multirate digital transmission. Several kinds of noises can exist in programmable high gain SC equalizers, such as switching noise, dc offset jump and transient response. In order to avoid their effects, a new adaptive SC filter is proposed. Two identical SC circuits are used in parallel. An input signal is fed into both SC circuits, and output signals from both circuits are alternately sent after the above noises are eliminated. Furthermore, many different data rates can be handled by slightly modifying an equalizer circuit. A bridged-tap echo canceller and a dc offset canceller are modified so as to be applied to the proposed adaptive SC filter.

A line equalizer system, which handles data rates ranging from 3.2 to 64 kbps, was designed. An LSI was fabricated using a 3-μm CMOS process. Experimental results show that noise effects are mostly eliminated, and frequency responses and eye openings are close to the designed values.

The proposed approach can expand applications of adaptive SC filters, particularly in continuous-time communication and signal processing.

I. Introduction

SWITCHED-CAPACITOR (SC) circuit techniques are very important in integrating many analog circuits on a monolithic LSI circuit [1]–[3]. Particularly, when high speed operation and low power dissipation are required, SC circuits play a very important role [4]. Recently, adaptive SC line equalizers have been applied to digital transmission over subscriber loops [5]–[7]. In these cases, high transfer gains, 40–50 dB, and high clock frequencies up to several megahertz are required.

Adaptive SC filters are usually constructed with programmable capacitor arrays (PCA's). Their characteristics are digitally controllable [8]–[10]. Programmable SC filters, however, cause undesired phenomena at the instant of changing filter responses. They include, for instance, switching noise, dc offset jump and transient response. These noises greatly degrade transmission quality. For this reason, SC line equalizers have been applied only to a ping-pong transmission system [11], in which noise effects can be avoided by changing PCA's during an equalizer pause interval.

Another technique to suppress the above mentioned noises is to slowly change SC circuit characteristics, using fractional capacitors. When high transfer gain is required, however, flat gain should be divided into several blocks, in order to compress a capacitance ratio range and to improve a signal-to-noise ratio. The divided flat gain is usually adjusted by relatively large gain steps. Furthermore, this approach cannot guarantee arbitrary filter responses.

The purpose of this work is to expand adaptive SC circuit applications to continuous-time communication and signal processing. For this purpose, a new adaptive SC filter is proposed, which can eliminate effects of the above noises. It consists of two identical variable SC circuits in parallel. An input signal is fed into both SC circuits, and output signals from both circuits are alternately sent to the next section, after the above-mentioned noises are eliminated.

By using the proposed approach, a line equalizer system, which can be applied to four-wire full-duplex digital transmission over subscriber loops, was designed and fabricated on a single-chip CMOS LSI. Algorithms and circuit realizations for a bridged-tap echo canceller and a dc offset canceller were modified from those for ping-pong transmission systems. An LSI was fabricated, using a 3-μm CMOS process, resulting in good performances.

II. Adaptive SC Filters

A. PCA's

Fig. 1 shows an example for a programmable SC filter, based on a stray insensitive integrator [12]. Capacitors are classified into three categories, sampling capacitor (C_{11}, C_{12}), coupling capacitor (C_{13}) and integrating capacitor (C_{10}). In order to continuously change a filter response, charge in PCA's should be continuous at the instant of changing branch capacitor combinations. This can be satisfied by changing sampling capacitors during a charging period, and connecting nonselected branch capacitors in integrating and coupling capacitors to the ground.

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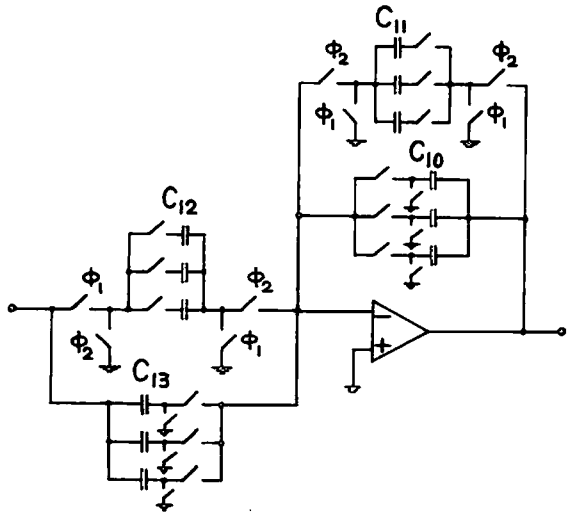


Fig. 1. Example for programmable SC filter.

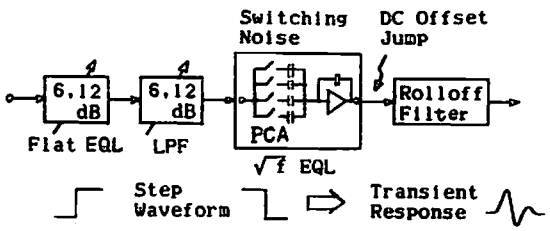


Fig. 2. Undesired phenomena in adaptive SC line equalizer.

B. Undesired Phenomena

Fig. 2 briefly illustrates three kinds of noises in an adaptive SC line equalizer system. When a high transfer gain is required, flat gain should be divided into several blocks, in order to compress a capacitance ratio range and to improve a signal-to-noise ratio [13]. In this example, flat gain is dispersed into a flat EQL, a low-pass filter (LPF) and $\sqrt{f}$ EQL. Flat gain in each block is adjusted by relatively large gain steps, such as 6 dB.

Switching Noise: Even though the branch capacitors are connected so as to guarantee capacitor charge continuity, impulsive noises could be caused through parasitic capacitors of MOS FET switches at the instant of changing PCA's.

Transient Response: Although the total gain is gradually adjusted, flat gain in each block varies by 6 dB, as shown in Fig. 2. Therefore, the blocks output becomes a step waveform in an instant. There actually exist some delay time between the adjoining blocks, due to finite response time. This causes impulsive noise. Furthermore, when the step waveform is bandlimited, before being adjusted by the complementary flat gain, a transient response, such as overshoot and undershoot, would occur.

DC Offset Jump: In SC circuits, dc offset is caused by operational amplifiers and clock feedthrough. The output dc offset is determined by both magnitude of dc offset sources and dc transfer gains from noise sources to the SC circuit output. The dc transfer gains depend on SC filter responses. Furthermore, there are many factors determining clock feedthrough, for instance, parasitic capacitors, integrating and sampling capacitors, and clock waveforms [1]. For this reason, the output dc offset is usually discontinuous at the instant of changing a filter response.

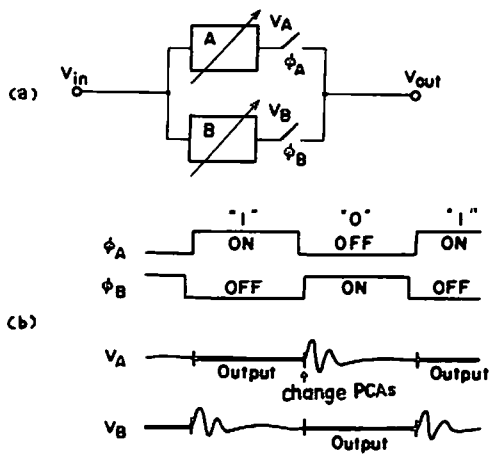


Fig. 3. Duplex structure adaptive SC filter. (a) Block diagram. (b) Timing chart.

III. New Adaptive SC Filter

Fig. 3 illustrates a basic structure and a timing chart for the proposed adaptive SC filter. Blocks A and B are synthesized by using variable SC circuits with PCA's. They have the same circuit configuration and the same element values.

An input signal v_{in} is fed into both blocks. Output signals v_A and v_B are sent v_{out} alternately through switches controlled by clocks ϕ_A and ϕ_B. During a period ($\phi_A = 1$), v_A is sent to v_{out}, and PCA's in the block B are changed. Impulsive and transient noises naturally attenuate, and dc offset deviation can be suppressed by using an offset canceller, during a period $\phi_B = 0$. After the undesired phenomena in the block B are eliminated, the output is switched from v_A to v_B. By alternating the output signals after eliminating the noises, an overall transfer response from v_{in} to v_{out} is completely identical to that for a single variable SC circuit without noise effects.

An example for the duplex SC circuit is illustrated in Fig. 4. The output signals from the blocks A and B are selected by an SC sample-and-hold (SH) circuit. Alternation between v_A and v_B is controlled by clocks ϕ_{iA} and ϕ_{iB}, $i = 1,2$. In order to continuously vary the output signal v, a charge corresponding to the output voltage v_B (v_A) is stored in the capacitor C_B (C_A) during the period $\phi_A = 1$ ($\phi_B = 1$).

Although the proposed adaptive SC filter requires double hardware size, it can be simplified by constructing both variable SC circuits in a time division multiplex (TDM) structure. An example for a TDM SC circuit will be given in Section V.

IV. Line Equalizer System

A. System Specifications

A line equalizer system, described in this paper, is used for four-wire full-duplex digital transmission over subscriber loops. Transmitted signal is bipolar coded data.

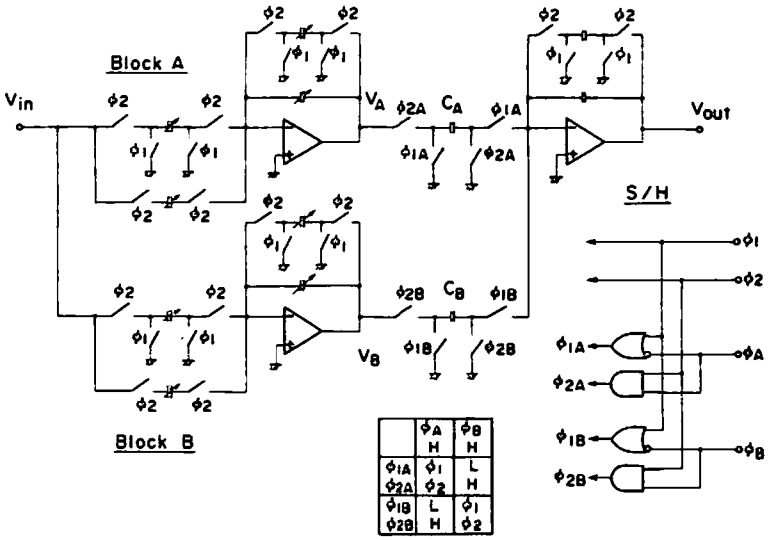


Fig. 4. Example for duplex SC circuit. Output alternation is controlled by ϕ_A and ϕ_B.

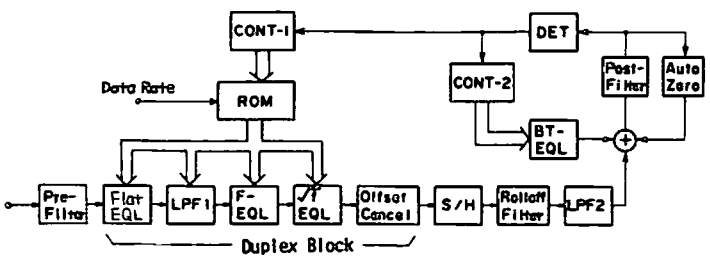


Fig. 5. Block diagram for adaptive SC line equalizer system.

Four kinds of data rates ranging from 3.2 to 64 kbps, are taken into account. Echos reflected from the bridged-taps, whose output terminal is opened, and output dc offset need to be thoroughly suppressed. An adjustable line loss at the Nyquist frequency is up to 44 dB. Eye openings are required to be more than 80 percent for all line lengths.

B. Block Diagram

Fig. 5 shows a block diagram for the developed line equalizer system. LPF1 and LPF2 are third-order SC low-pass filters, which are used for decimation and interpolation, respectively. A pre-filter and a post-filter are second- and third-order active *RC* low-pass filters, respectively. LPF1 also serves as a flat gain equalizer having 6- and 12-dB gain steps. The equalizer consists of a course $\sqrt{f}$ EQL and a fine (*F*-) EQL. Since these equalizers have 16 kinds of discrete responses, 256 kinds of responses can be realized as a whole. A differential gain between the adjoining responses becomes 44 dB/256 $\simeq$ 0.2 dB. A rolloff filter is a fourth-order SC filter, which is designed to have 100 and 200 percent raised cosine amplitude responses for high and low data rates, respectively. The adaptive blocks from the flat EQL to the offset canceller is fully duplexed in the same way as the adaptive SC circuit shown in Figs. 3 and 4.

A sampling frequency for the equalizer is determined to be four times as high as each data rate in order to compress a capacitance ratio range. Analog pre-filter and post-filter, which usually occupy a large chip area, can be simplified by operating LPF1 and LPF2 with a high clock frequency.

Two kinds of dc offset cancellers are used at the $\sqrt{f}$ EQL output and the post filter output. A bridget-tap echo canceller, called BT-EQL in Fig. 5, is employed at the post filter output. Control signals for BT-EQL coefficients are generated in CONT-2. Residual echos at data sampling points are detected in DET. The peak value for the post-filter output is also detected by DET. PCA control signals are generated in CONT-1 and are decoded by a read-only memory (ROM).

Detailed descriptions on adaptation algorithm and circuit realization for each block will be given in Sections V and VI.

V. Equalizer Design

A. Circuit Configuration

A simple way for modifying an SC equalizer circuit, to be applied to multi-rate data transmission, is to change its clock frequency. Line loss characteristics for different data rates are, however, not exactly the same as those obtained by frequency shifting. Therefore, the equalizer responses, obtained by changing a clock frequency, should be further optimized by changing capacitance ratios. This means, however, increasing in memory capacity for PCA control signals.

In this paper, the $\sqrt{f}$ EQL is divided into two equalizers $\sqrt{f}$ EQL-1 and $\sqrt{f}$ EQL-2, which realize the major part and the minor part of $\sqrt{f}$ characteristics, respectively.

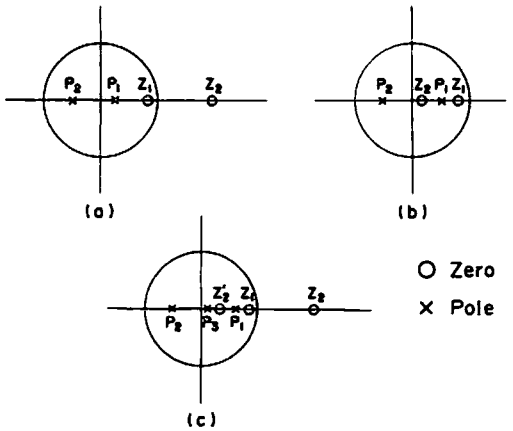


Fig. 6. Pole-zero locations for $\sqrt{f}$ EQL.

Furthermore, data rates are classified into high-rate and low-rate groups. The clock frequency is tuned to all data rates.

Since a large number of capacitors and a wide capacitance ratio range are required in $\sqrt{f}$ EQL-1, the number of capacitors to be prepared for data rates should be minimized. For this purpose, capacitance ratios in $\sqrt{f}$ EQL-1 are changed only for high- and low-rate groups. The residual errors in each group are compensated for by modifying capacitance ratios in $\sqrt{f}$ EQL-2 for all data rates.

B. Pole-Zero Location

A $\sqrt{f}$ EQL transfer function is approximated in a time domain, so as to minimize the intersymbol interference for an isolated pulse response obtained by passing a 50-percent duty pulse through a line and the entire equalizer system. Capacitances are further discretely optimized, using pole-zero deviation as an error criterion [13].

Two kinds of pole-zero locations, shown in Fig. 6, result. For the low-rate group, a pole-zero location (b) is optimum for all line lengths. On the other hand, in the high-rate group, pole-zero locations (a) and (b) become optimum for long and short line lengths, respectively. If the pole-zero location is switched between (a) and (b) at a certain gain level, the delay time of $\sqrt{f}$ EQL rapidly changes. This causes a synchronization error for the optimum sampling point.

For this reason, the combined pole-zero location (c) is employed for the equalizer transfer function. Furthermore, the pole-zero location (a) or (b) is assigned to $\sqrt{f}$ EQL-1, while the remainder is used for $\sqrt{f}$ EQL-2.

C. TDM Realization

Parallel SC circuits can be simply realized in a TDM structure [14]. A TDM circuit configuration and a timing chart for SC circuits from F-EQL to the SH circuit are shown in Fig. 7. Since sampling capacitors are discharged at each clock period, they can be basically used by both SC circuits. However, since signals passing through C_{13} and C_{22} in $\sqrt{f}$ EQL-1 should be delayed by one clock, these capacitors must be independently prepared for each SC circuit. Therefore, 4-phase clocks ϕ_{1a}, ϕ_{2a}, ϕ_{1b}, and ϕ_{2b} are employed. Since integrating capacitors C_{10} and C_{20} and a coupling capacitor C_{11} always hold charge, they are not multiplexed, and must be prepared in parallel.

In the timing chart, shaded portions of F-EQL and $\sqrt{f}$ EQL outputs are transfered to the next section. The other parts, denoted with dotted lines, are stored in the integrating capacitors.

D. Effects of Mismatches between Duplexed SC Circuits

In actual LSI fabrication, mismatches between parallel SC circuits are unavoidable. Mismatches include, for instance, deviations in operational amplifier performances, capacitance ratios, parasitic capacitances in FET switches and so on. In the TDM structure, however, operational amplifiers and some of the sampling capacitors are commonly used by both SC circuits. Noise effects do not appear at the duplex SC circuit output. Furthermore, MOS technology can achieve highly accurate capacitance ratios. Deviations in SC line equalizer characteristics can be expected to be less than 0.2 dB, which is the minimum gain step. Taking these situations into account, effects of mismatch between the duplex SC circuits could be negligible.

VI. Other Building Blocks

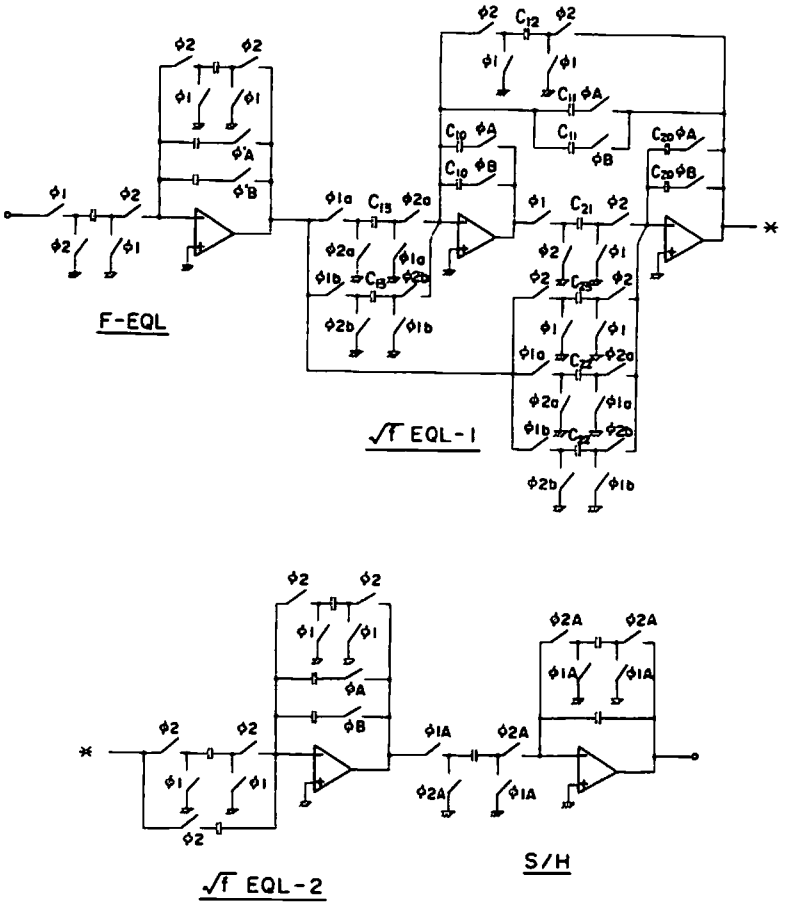
A. Programmable Capacitor Arrays

One efficient approach to constructing PCA's is to use differential capacitors between the adjoining filter responses as branch capacitors [7]. However, in the case of multi-rate data transmission, differential branch capacitors should be prepared for each data rate. Thus, PCA's become very complicated. For this reason, binary weighted PCA's are adopted. Control signals for PCA's are stored in ROM. In order to simplify control signals and to minimize the total capacitance, PCA's include the minimum capacitor as a fixed branch capacitor in parallel.

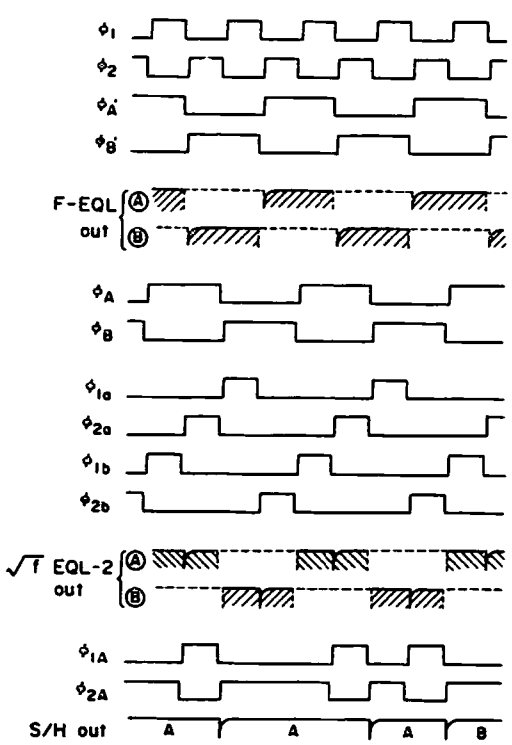
B. Gain Control Circuit

An equalizer response is controlled so that the peak value of the post-filter output approaches the reference voltage. The $\sqrt{f}$ equalizer characteristics are designed so as to exactly compensate for the line loss characteristics, when the peak value is equal to the reference value. This peak adjusting method cannot guarantee an optimum equalizer response, when there exist flat gain deviations. Furthermore, since a typical line diameter is only taken into account in approximating the $\sqrt{f}$ equalizer, different diameter lines also cause mismatch. The intersymbol and interference caused by those mismatches are mainly concentrated within $2T$ after the main pulse, where T is a data sampling period. It can be compensated for by the bridged-tap echo canceller, as described in the next section.

In Fig. 5, the post-filter output peak is detected in DET. An 8 bit up/down counter, included in CONT-1, outputs equalizer gain levels from 0 to 255. This counter is incremented or decremented as the number of data, whose peak value exceeds the reference voltage, is greater or less than



(a)



(b)

Fig. 7. Time division multiplex realization for SC circuits from F-EQL to SH circuit. (a) Circuit configuration. (b) Timing chart.

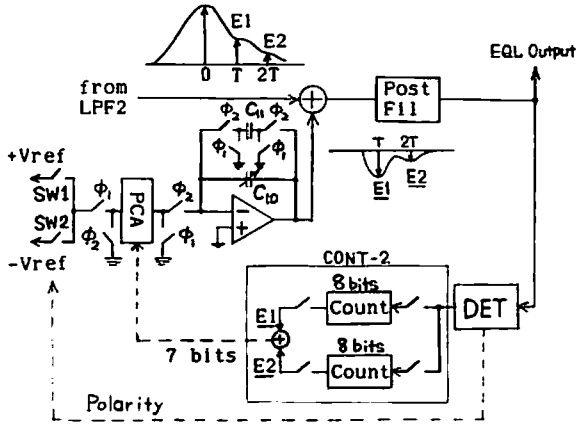


Fig. 8. Bridged-tap echo canceller.

half of all incoming data, respectively. The CONT-1 output is decoded by ROM into binary code used for controlling PCA's. ROM is further addressed by the external signal expressing data rate.

C. Bridged-Tap Echo Canceller

Echos, reflected from bridged-taps, whose output terminal is opened, significantly degrade data transmission quality. Therefore, a decision feedback equalizer, BT-EQL in Fig. 5, has been employed [6]. Conventional approaches expect a specific bit pattern "$0X00$" ($X=1$ or -1) with some statistical probability. In this case, BT-EQL coefficients are directly controlled by samples at T and $2T$. There are, however, many situations, where the above bit pattern is not expected to appear so often, and a bipolar rule is not always guaranteed, particularly in four-wire data transmission.

In this paper, a BT-EQL algorithm is further modified so as to be applied to a more general case. A block diagram for the bridged-tap echo canceller is given in Fig. 8. BT-EQL coefficients $E1$ and $E2$, which correspond to echo peaks $E1$ and $E2$, are supplied by two 8 bit up/down counters, included in CONT-2. $E1$ is renewed when a bit pattern "$X0$" is received, by using a sample at T. When a bit pattern "$0X00$" comes, $E2$ is renewed using a sample at $2T$. $E1$ and $E2$ are transfered through the switches and converted into analog waveforms through the SC LPF and the post-filter. Thus, the SC LPF serves as both a D/A converter and a waveform shaping filter. The polarity is controlled by switches SW1 and SW2.

Since the post-filter cutoff frequency is fixed, a clock frequency for the SC LPF is also fixed. Therefore, the SC LPF cutoff frequency, which controls rising and falling times, is tuned to each data rate by changing the capacitance C_{10}. $E1$ and $E2$ should be less than about 50 percent of the main pulse peak value, in order to guarantee stable BT-EQL operation, even though the bipolar rule is not satisfied. Requirement for echo cancellation in four-wire digital transmission are usually less than 50 percent of the peak value.

In the initial settling interval, the $\sqrt{f}$ equalizer is first adjusted. After that, BT-EQL is adjusted on receiving the bit patterns "$X0$" and "$0X00$". After both equalizers are settled, the $\sqrt{f}$ equalizer is modified at some interval, and the BT-EQL coefficients $E1$ and $E2$ are renewed in the same way as in the above.

Computer simulation for a BT-EQL convergence process is shown in Fig. 9. Initial echos at T and $2T$ are 30 percent and 10 percent of the main pulse, respectively. Solid and dotted lines indicate residual echos at T and $2T$, respectively. A random bit pattern with a 1/8 mark rate is used. This figure shows BT-EQL settles down after $250T$.

D. DC Offset Canceller

A block diagram for two kinds of dc offset cancellers is shown in Fig. 10. Since, in the duplex SC circuits, dc offset must be suppressed before alternating the output signals, an offset canceller should be prepared for each block.

During a period ($\phi_A=1, \phi_B=0$), the input terminal of the block B and a capacitor C_B are connected to the ground. DC offset in the block B is integrated in C_B through a first-order SC LPF, which consists of capacitors C_B and C_B', and switches controlled by clocks ϕ_1 and ϕ_2. After switching noise and transient response in the block B vanish, the switching state is changed from ($\phi_A=1, \phi_B=0$) to ($\phi_A=0, \phi_B=1$). The block B output signal is transfered to the SH circuit through switches controlled by the clock ϕ_B. At the same time, the dc offset stored in C_B is subtracted from the output signal. In this period, dc offset in the block A is integrated in C_A.

DC offset caused in the fixed block from the S/H circuit to the post-filter is detected and fed back to an SC adder through an integrator. The integrator consists of a set of p-ch and n-ch transistors and an integrating capacitor C. When the gate voltage exceeds some preconceived level, a transistor operates in the saturation region. This means the transistor serves as a current source, and charges or discharges the capacitor C. A pulse generator, in the offset detector, provides an appropriate polarity pulse, according to the detected dc offset polarity. Pulse width determines an integrator time constant.

Features of these approaches are to avoid an RC integrator, which usually occupies a large chip area, and to be applied to different kinds of data rates only by changing a clock frequency.

VII. LSI Implementation

A. LSI Design

A line equalizer system was designed, and an LSI was fabricated. Device technologies are double layer poly-silicon, double layer aluminum wiring and silicon gate CMOS process with 3-μm channel length. There are 3500 gates in a digital portion, and ROM capacity is 1300 bits for each data rate. An analog portion includes 25 operational amplifiers, 8 comparators and 3400 unit capacitors. Unit capacitances are 0.1 and 0.2 pF for BT-EQL and other SC circuits, respectively.

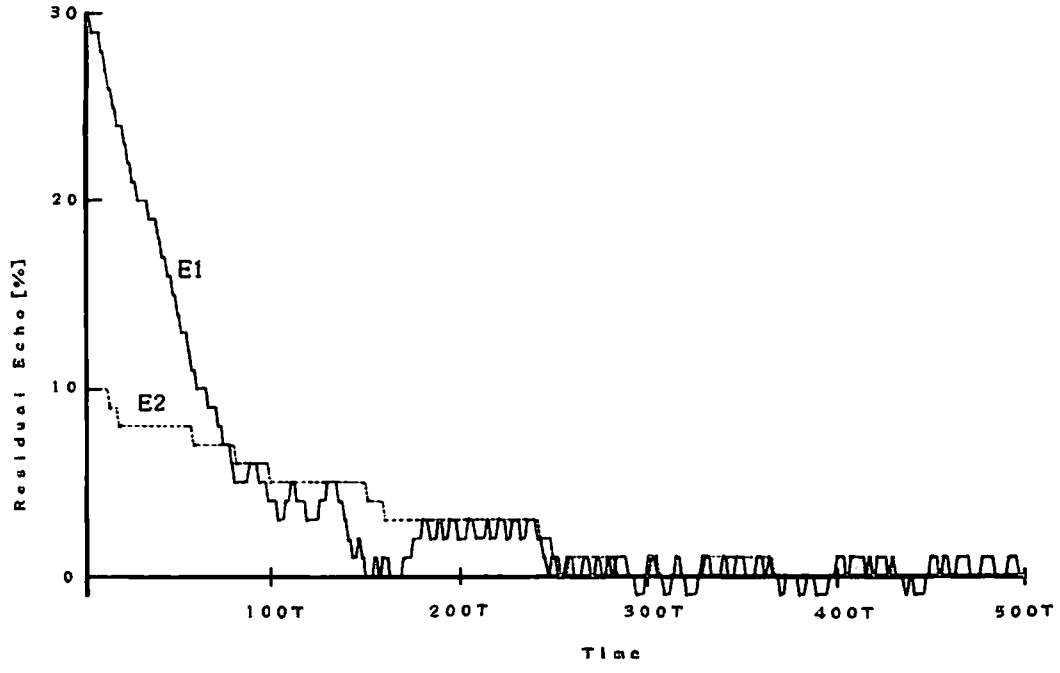


Fig. 9. Convergence process in bridged-tap echo canceller. Solid and dotted lines indicate residual echos at T and $2T$, respectively.

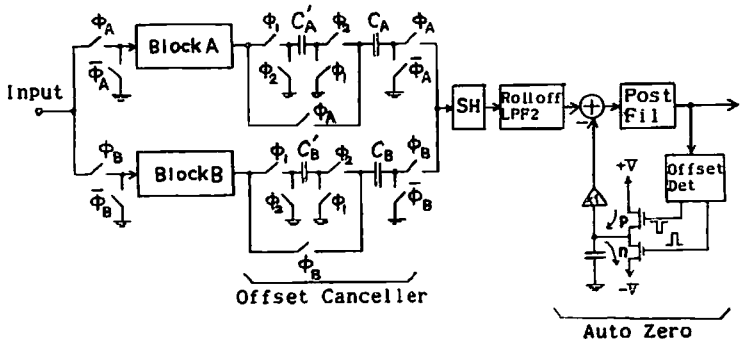


Fig. 10. DC offset cancellers for duplex block and fixed block.

LPF1 operates with a high sampling frequency, which is 16 times as high as each data rate, and is synthesized in a TDM structure. Its clock frequency becomes 2.048 MHz for 64 kbps. Furthermore, the equalizer amplifies various kinds of noises, as well as the received signal. Therefore, operational amplifiers are required to achieve high speed operation, a high power supply rejection ratio (PSRR) and low power dissipation. For this purpose, a two stage configuration, consisting of a differential input stage and a common source stage, is employed. Designed performances are 70-dB dc gain, 13-MHz unity gain frequency, 130-ns settling time, and more than 60-dB PSRR.

In order to further improve PSRR in SC circuits, ratios of stray capacitances and integrating capacitances are decreased. Furthermore, since a small size transistor forms a first-order RC low-pass filter with a relatively low cutoff frequency, high frequency noise can also be suppressed.

An LSI microphotograph is shown in Fig. 11. Chip area is 45.5 mm^2, where 44 percent is a digital portion including ROM, 7 percent is capacitor arrays, 38 percent is a wiring space, and other blocks occupy 11 percent of the chip area. Power dissipation is 190 mW with a single +5 V power supply.

B. Experimental Results

Amplitude responses for an entire equalizer system are shown in Fig. 12. The data rate is 64 kbps. Solid lines indicate designed responses, and black specks indicate the measured data. Their differences are very small. Fig. 13 illustrates eye openings for 3.2 kbps (19-km line lengths), 12.8 kbps (11 km), and 64 kbps (6 km). The measured eye openings for all data rates and line loss up to 44 dB are more than 80 percent. From the measured eye pattern, it can be confirmed that the effects of undesired phenomena are mostly eliminated. DC offset voltage for an entire system is less than 4 mV, which can be negligible in actual applications. PSRR is 50 dB for the maximum gain step.

VIII. Conclusion

A new adaptive SC filter has been proposed, which is free from the effects of several kinds of noises. It has been applied to a line equalizer system, which can be used in

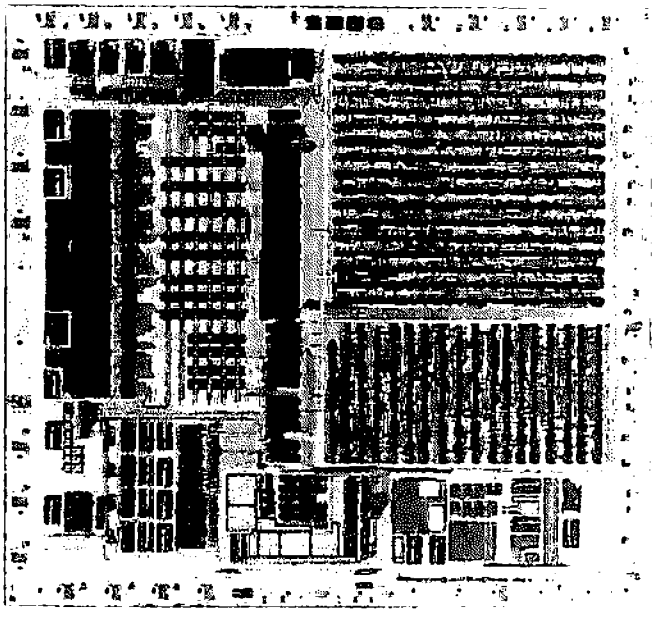


Fig. 11. Microphotograph for line equalizer system LSI.

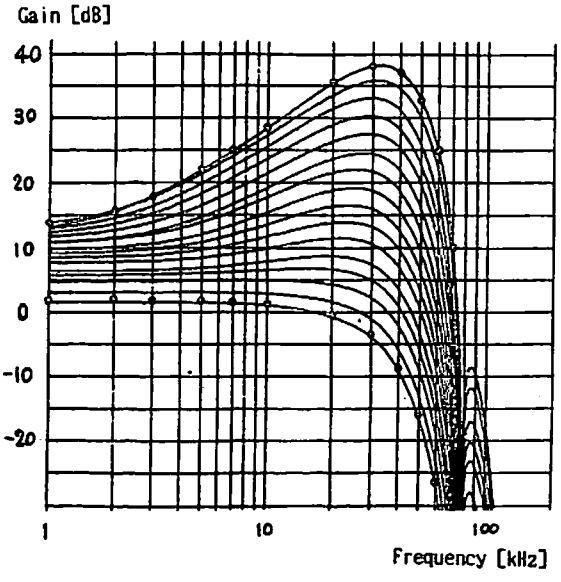


Fig. 12. Amplitude responses for a whole line equalizer system. Solid lines and ∘ indicate designed and measured amplitude responses, respectively.

four-wire full-duplex and multi-rate digital transmission over subscriber loops. The bridged-tap echo canceller and the dc offset canceller have been further improved from the conventional circuits. An LSI was fabricated using a 3-μm CMOS process, resulting in good performances in regard to both frequency and time responses. Noise effects are mostly eliminated.

The proposed adaptive SC filter can expand its applications, particularly in continuous-time communication and signal processing.

Acknowledgment

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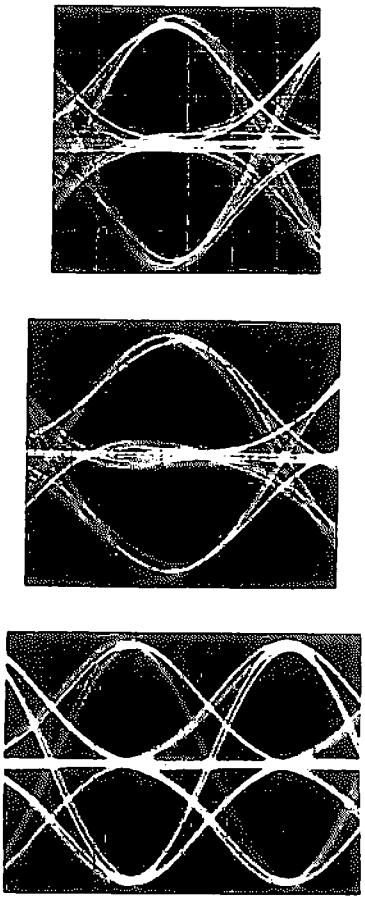

Fig. 13. Measured eye openings for 3.2 kbps (19-km line lengths), 12.8 kbps (11 km), and 64 kbps (6 km).

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