A single-chip SC line equalizer system for full duplex multi-bit rate digital transmission

メタデータ	
	言語: eng
	出版者:
	公開日: 2017-10-03
	キーワード (Ja):
	キーワード (En):
	作成者:
	メールアドレス:
	所属:
URL	http://hdl.handle.net/2297/6827

A SINGLE-CHIP SC LINE EQUALIZER SYSTEM FOR FULL DUPLEX MULTI-BIT RATE DIGITAL TRANSMISSION

Kenji NAKAYAMA, Yutaka TAKAHASHI, Yayoi SATOH, Masahiro NAKA
and Yasuaki NUKADA

NEC Corporation
Miyamae-Ku, Kawasaki 213 JAPAN

ABSTRACT

This paper presents a single-chip SC line equalizer system, which can be applied to full duplex digital transmission. Adaptive SC filters, constructed with programmable capacitor arrays (PCAs), usually cause undesired responses, such as spike noise and transient response, which degrade data transmission quality. In order to avoid these phenomena, a duplex SC equalizer is introduced, which has the same circuits in parallel. PCAs in one duplex equalizer, whose output is not transfered, are varied. After the undesired phenomena vanish, the output is alternated. The equalizer system can be applied to several different bit rates,merely by changing the external control signals. An algorithm for a bridged tap echo canceller is modified for a more general case. A DC offset canceller and an auto zero circuit are employed for variable and fixed blocks, respectively. A line equalizer system was designed for four different bit rates, ranging from 3.2 to 64 kbps, and an LSI was fabricated using a $3 \mu m$ CMOS process. Chip area is 45.5 mm², and power dissipation is 190 mW with a single +5V power supply.

INTRODUCTION

Switched capacitor (SC) circuit techniques are very useful to integrate analog signal processing systems [1]. One hopeful application field is high speed data transmission over subscriber loops [2]. In this case, an adaptive line equalizer is an important function to achieve high data transmission quality.

Adaptive SC filters are constructed with programmable capacitor arrays (PCAs) [3], and their response is discretely varied. Since an equalizer gain is high, for instance 40-45 dB at the Nyquist frequency, it should be divided into several blocks, in order to compress capacitance ratios in the SC circuits [4]. Therefore, in the instant of changing the equalizer gain, spike noise and transient response occur. These undesired phenomena degrade data transmission quality. For this reason, existing SC line equalizer systems have been restricted to time-shared two-wire digital transmission [5]-[7].

However, in the case of full duplex four wire digital transmission, an adaptive SC equalizer is required to be free from the above phenomena. Furthermore, using this kind of adaptive SC filter can expand application fields.

In this presentation, a duplex structure SC filter is proposed to overcome the above problems. Stress will be also placed on how to synthesize an SC line equalizer, which can be applied to different frequency bands by simple modification. Algorithms and circuit realizations for a bridged tap echo canceller and a DC offset canceller

are further improved. An LSI, which is applied to four-wire digital transmission and four kinds of bit rates, was designed and fabricated using a $3 \mu m$ CMOS process.

DUPLEX STRUCTURE ADAPTIVE SC FILTER

Undesired Responses
Spike Noise:
In the instant of switching PCAs, charge stored in unselected branch capacitors, and leakage charge through stray cpacitors cause spike noises.
Transient Responses:
Since capacitance ratios in an SC equalizer are proportional to a gain at the Nyquist frequency, which is usually 40-45 dB, the gain is divided into other blocks by 6 or 12 dB [4]. These large gain steps generate a step waveform. If the step waveform is band limited in the successive blocks, a transient response will occur.
DC Offset:
DC offsets are caused by operational amplifiers and clock feedthrough. A DC offset, which appears at the output, varies in accordance with the equalizer response.

Duplex Structure SC Filter
A block diagram and a timing chart for the proposed duplex SC filter are illustrated in Fig.1. Blocks A and B are variable SC circuits having the same configuration. Input signal v_{in} is fed to both blocks, their output signals v_A and v_B are transfered to v_{out} alternately. During the period when v_A is transfered to v_{out}, block B characteristics are changed. After undesired responses in block B are eliminated, the output is switched from v_A to v_B. By alternating the output in the steady state, a complete transfer response, from v_{in} to v_{out}, is equivalent to that of a single variable SC circuit.
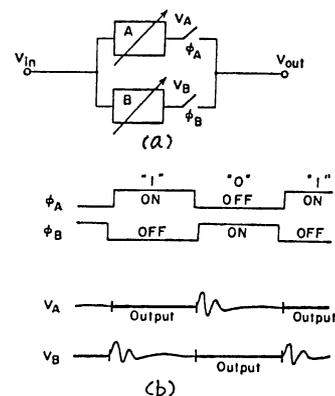

Fig.1. Duplex structure of variable SC circuit.
(a)Block diagram. (b)Timing chart.

One example for a duplex SC circuit is illustrated in Fig.2. The output signals from blocks A and B are selected by an SC sample & hold (S/H) circuit. Alternation between v_A and v_B is controlled by clocks ϕ_{iA} and ϕ_{iB}, i=1,2. In order to gradually vary the output signal v_{out}, a charge corresponding to v_B (v_A) is stored in C_B (C_A) during the time when $\phi_A=1$ ($\phi_B=1$).

Although a duplex SC circuit requires complicated hardware, it can be simplified by constructing SC circuits in a time division multiplex form.
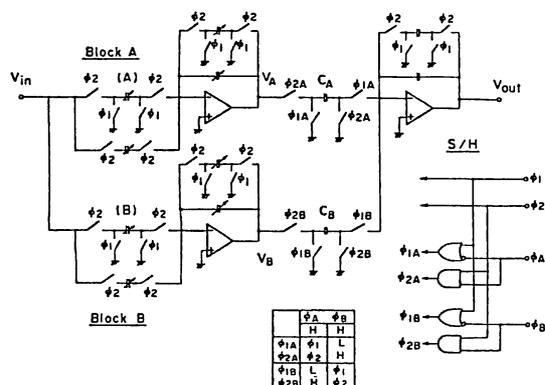

Fig.2. Example for duplex SC circuit. Output alternation is controlled by ϕ_A and ϕ_B.

LINE EQUALIZER SYSTEM

System Specifications

Several kinds of bit rates are taken into account. Bipolar coded data are transmitted over four wire in a full duplex mode. Echos from the bridged taps and DC offsets need to be thoroughly suppressed. Adjustable line loss at the Nyquist frequency is up to 44 dB. Eye openings are required to be more than 85 % for all gain steps.

Block Diagram

Figure 3 shows a block diagram for the proposed line equalizer system. LPF1 and LPF2 are 3rd-order SC lowpass filters, which are used for decimation and interpolation, respectively. A pre-filter and a post-filter are 2nd-order and 3rd-order RC lowpass filters, respectively. LPF1 flat gain values are changed by 6 and 12 dB. The equalizer consists of a course $\sqrt{f}$ EQL and a fine (F-) EQL, which have 16 step responses. Therefore, 256 step responses can be realized as a whole. A differential gain becomes 44 dB/ $256 \fallingdotseq 0.2$ dB [6]. A rolloff filter is designed to have a 100% raised cosine amplitude response.

Sampling frequencies for the $\sqrt{f}$ EQL and the roll-off filter are determined to be four times and eight times as high as each bit rate, respectively.

The peak value of the post-filter output is detected by DET. PCA control signals are generated by CONT-1 and a read only memory (ROM).
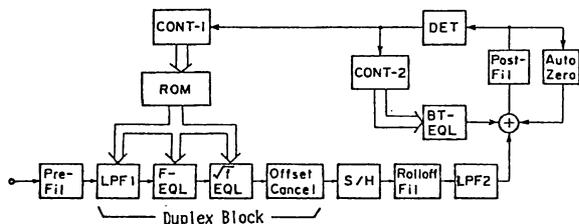

Fig.3. Block diagram for line equalizer system.

SC EQUALIZER DESIGN FOR MULTI-BIT RATES

Circuit Configuration

The simplest approach to modifying an SC equalizer circuit for multi-bit rate data is to change clock frequency. In this case, however, the equalizer characteristics are not well matched to the line loss. Another method is to modify a combination of two $\sqrt{f}$ EQLs [8]. Although this approach can provide efficient performances, control signals and a flat gain adjusting process become somewhat complicated.

For this reason, another approach is employed. The $\sqrt{f}$ EQL is divided into two equalizers, which realize a main part of the original $\sqrt{f}$ EQL and the remaining part. These equalizers are called $\sqrt{f}$ EQL-1 and $\sqrt{f}$ EQL-2, respectively. Bit rates are classified into high-rate and low-rate groups. In each group, the same $\sqrt{f}$ EQL-1 is used only by changing the clock frequency. $\sqrt{f}$ EQL-2 is slightly modified for each bit rate. $\sqrt{f}$ EQL-1 is changed for high-rate and low-rate groups.

Pole-Zero Locations

A transfer function of $\sqrt{f}$ EQL is approximated in a time domain, so as to minimize the intersymbol interference for an isolated pulse response. Capacitances are further discretely optimized, using pole-zero deviation as an error criterion [4].

Second-order and first-order transfer functions are assigned to $\sqrt{f}$ EQL-1 and $\sqrt{f}$ EQL-2, respectively. Two different kinds of pole-zero locations are shown in Fig.4. For the low-rate group, pole-zero location (b) is optimum in all gain steps. On the other hand, in the high-rate group, pole-zero locations (a) and (b) become optimum for high and low gain steps, respectively. Therefore, the combined pole-zero location (c) is employed in the transfer function approximation procedure. Pole-zero location (a) or (b) is assigned to $\sqrt{f}$ EQL-1. The remaining location is used for $\sqrt{f}$ EQL-2.
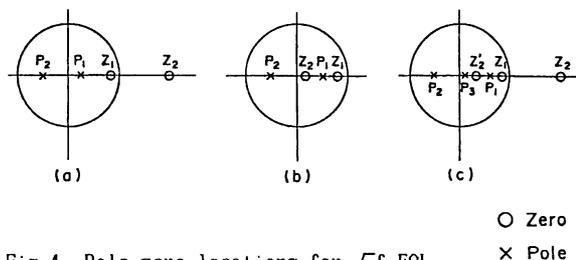

Fig.4. Pole-zero locations for $\sqrt{f}$ EQL.

HARDWARE REALIZATION

TDM Configuration

A TDM circuit configuration and a timing chart for the block from F-EQL to the S/H circuit are shown in Fig.5. Since sampling capacitors are discharged at each clock period, they can be basically shared between duplex circuits. However, in $\sqrt{f}$ EQL-1, C_{13} and C_{22} cannot be shared, because signals passing through them should be delayed by one clock. Integrating capacitors $C_{1\theta}$ and $C_{2\theta}$, and a coupling capacitors C_{11}, always hold a charge, and they are not multiplexed.

Programmable Capacitor Array

One efficient approach to constructing PCAs is to use differential capacitors between the adjoining gain steps
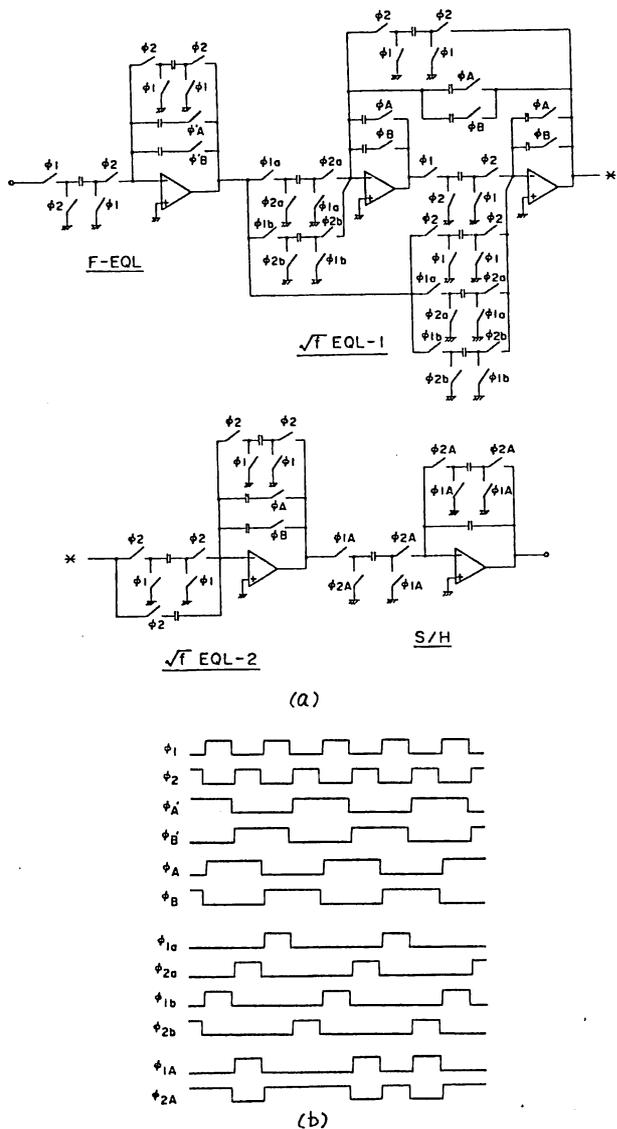
F-EQL

√f EQL-1

√f EQL-2

S/H

(a)

(b)

Fig.5. Time division multiplex realization for block from
F-EQL to S/H circuit. (a) Circuit configuration.
(b) Timing chart.

as branch capacitors. However, for processing multi-bit
rate data, branch capacitors should be prepared for each
bit rate. Therefore, binary weighted PCAs are adopted.
Control signals are stored in ROM. In order to simplify
control signals and to minimize the total capacitance,
PCAs contain the minimum capacitor as a branch capacitor.

Gain Control Circuit

The peak value of the post-filter output is compared
with five kinds of reference levels $\pm V_{ref}$, $\pm V_{ref}/2$ and 0
in DET. CONT-1 includes an 8 bit up/down counter, which
stores information for an equalizer gain level to be
realized. This counter is incremented and decremented at
several intervals, if a ratio for the numbers of data,
whose peak value exeeds V_{ref}, and all coming data is
greater and less than 1/2, respectively. The information
from CONT-1 is decoded by ROM into binary code used for
PCA control.

Bridged Tap Echo Canceller

Since echos, reflected from bridged taps, whose output
terminal is opened, significantly degrade data trans-
mission quality, a decision feedback equalizer, called BT-
EQL in Fig.3, has been employed [6]. The conventional
approaches expect that a specific bit pattern "0X00" (X=1
or -1) would occur with some statistical probability. In
this case,tap gains at 1T and 2T seconds (E_1 and E_2) after
the main pulse, where T is one period of a bit rate, are
controlled by samples obtained from the pulse train "0X00"

In this paper, a more general case is considered, where
the above bit pattern is not expected so often, and a bi-
polar rule is not always guaranteed. In the proposed
method, tap gains E_1 and E_2 are controlled by the samples
obtained from bit patterns "X0" and"0X00",respectively.

E_1 and E_2 are stored in two 8 bit up/down counters
included in CONT-2, and converted into an analog signal by
an SC circuit shown in Fig.6. Switches SW_1 and SW_2 control
the polarity of V_{ref} and timing for the counter output.
The 1st-order SC LPF is used for waveform shaping. Capaci-
tor C_{18} is varied to justify a cutoff frequency in accord-
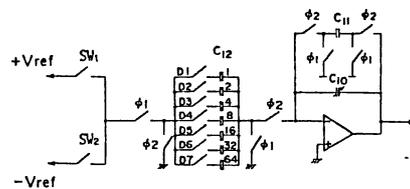ance with the bit rate.

Fig.6. SC circuit for BT-EQL consists of 7 bit PCA and LPF

DC Offset Canceller

DC offsets caused in SC circuits compress eye opening,
and degrade the noise margin.

In the duplex circuit, DC offsets must be suppressed
before alternating the outputs. Therefore, an offset can-
celler is included in each block. By connecting the input
terminal to the ground, the DC offset is extracted as the
√f EQL output. The DC offset is sampled, and is sub-
tracted from the signal. DC offset caused in the fixed
block from the S/H circuit to the post-filter is fed back
through an RC integrater to an SC adder. This kind of off-
set canceller is called an "auto zero" circuit [9]. A
resistor in the integrater is realized with an on-resistor
of a MOS transistor. By shortening a transistor on time, a
large resistance value can be equivalently realized with
a small chip area.

LSI IMPLEMENTATION

LSI Design

A line equalizer system was designed, and an LSI was
fabricated. Four kinds of data rates, from 3.2 to 64 kbps,
are taken into account. Device technologies are double
layer poly-silicon, double layer aluminum wiring and sili-
con gate CMOS process whose channel length is 3 μm. There
are 3500 gates in a digital portion, and ROM capacity is
1300 bits. An analog portion includes 25 operational
amplifiers, 8 comparators and 3400 unit capacitors. Unit
capacitances are 0.1 pF and 0.2 pF for BT-EQL and other SC
circuits, respectively.

Since LPF1 operates with a sampling frequency 16 times
as high as a bit rate and is duplexed, its clock frequency
becomes 2.048 MHz for 64 kbps. Furthermore, the equalizer
amplifies various kinds of noises, as well as the received
signal. Therefore, operational amplifiers were designed so
as to achieve high speed operation, a high power supply

29. 2. 3

rejection ratio (PSRR) and low power dissipation. A two
stage configuration, consisting of a differential input
stage and a common source stage, is employed. Designed
performances are 70 dB DC gain, 13 MHz unity gain fre-
quency, 130 nSec settling time, and more than 60 dB PSRR.

In order to further improve PSRR in SC circuits, ratios
of stray capacitances and integrating capacitances should
be minimized. For this purpose, integrating capacitances
are designed as large as possible, and analog switches are
designed as small as possible. Furthermore, a small size
transistors forms a 1st-order RC lowpass filter, which can
suppress high frequency noise.

A chip area is 45.5 mm², where 44% is a digital portion
including ROM, 7% is the capacitor arrays, 38% is the
wiring space, and other blocks occupy 11% of the area. A
microphotograph of the line equalizer LSI is shownin Fig.7
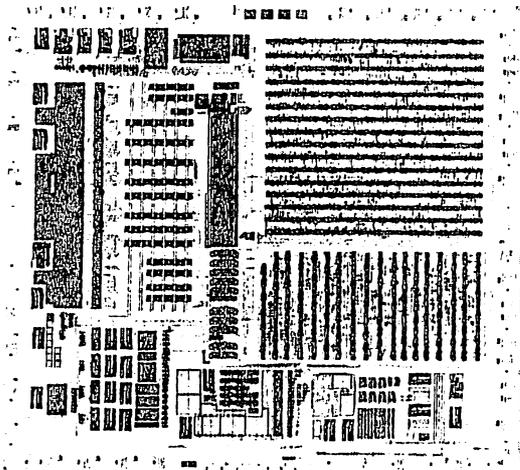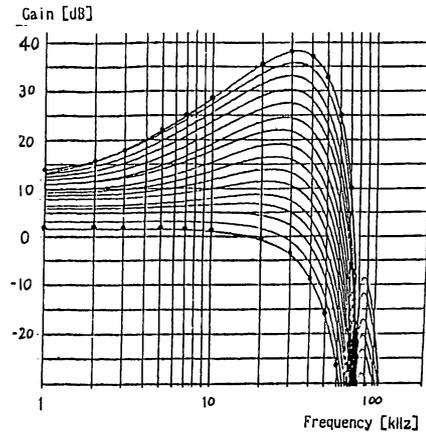Power dissipation is 190 mW with a single +5V power supply.

Fig.8. Amplitude responses for block from pre-filter to
post-filter. Solid lines and ● indicate designed and
measured amplitude responses.

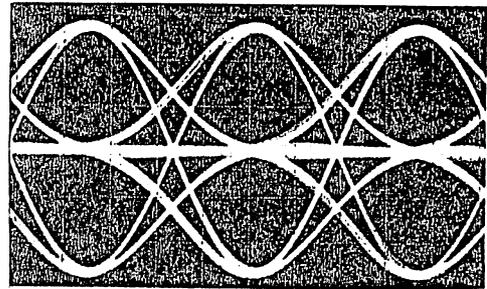Fig.7. Microphotograph for line equalizer LSI.

Fig.9. Measured eye opening for 64 kbps. Line length is
5.9 km and line loss is 34 dB at 32 kHz.

Experimental Results

Measured data for 64 kbps are briefly presented here.
Amplitude responses are shown in Fig.8. Figure 9 shows
an eye opening, where a line length is 5.9 km, and a line
loss is 34 dB at the 32 kHz Nyquist frequency. Those
results are close the designed values. DC offset voltage
for a whole system is less than 4 mV, which can be negli-
gible in actual applications. PSRR is 50 dB for the maxi-
mum gain step.

CONCLUSION

Design techniques for an SC line equalizer system have
been proposed. The system can be applied to full duplex
digital transmission and multi-bit rate data. An equal-
izer system was designed, and an LSI was fabricated using
a 3 μm CMOS process. Experimental results indicate the
proposed technique efficiency. The proposed adaptive SC
filter could be useful in a wider range of application
fields.

ACKNOWLEDGEMENT

REFERENCES

[1]R.Gregorian, K.Martin and G.C.Temes,"Switched-capacitor
circuit design", Proc. IEEE vol.71 pp.941-966, Aug. 1983.
[2]N.Inoue, R.Komiya and Y.Inoue,"Time-shared two-wire
digital subscriber transmission system and its application
to the digital telephone set," IEEE Trans. Commun.,vol.COM
-29,pp.1565-1572, Nov. 1981.
[3]K.Martin and A.S.Sedra,"Switched-capacitor building
blocks for adaptive systems",IEEE Trans. Circuits Syst.,
vol.CAS-28, pp.576-584, June 1981.
[4]K.Nakayama, Y.Satoh and Y.Kuraishi,"Design techniques
for switched-capacitor adaptive line equalizer", IEEE
Trans. Circuits Syst., vol.CAS-32, pp.750-766, Aug. 1985.
[5]H.Takatori, T.Suzuki, F.Fujii and M.Ogawa,"A CMOS line
equalizer for digital subscriber loop", IEEE J. Solid-
State Circuits, vol.SC-19, pp.906-912, Dec. 1984.
[6]M.Ishikawa, T.Kimura and N.Tamaki,"A CMOS line
equalizer", IEEE J. Solid-State Circuits, vol.SC-19, pp.
788-793, Oct. 1984.
[7]Y.Kuraishi et al."A switched capacitor adaptive line
equalizer for a high-speed digital subscriber loop", in
Proc. Custom Integrated Circuits Conf., pp.264-268, 1984.
[8]K.Nakayama, Y.Satoh and Y.Okuyama,"On pole-zero
location in SC line equalizer (in Japanese)", IECE Japan,
National Convention Rec.,p.2085, Mar. 1985.
[9]A.Iwata et al.,"A single-chip codec with switched-
capacitor filters", IEEE J. Solid-State Circuits, vol.SC-
16, pp.315-321, Dec. 1981.

29. 2. 4