

Silicon Lateral Avalanche Photodiodes Fabricated by Standard 0.18 μm CMOS Process

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Abstract A Si APD was fabricated by standard 0.18 μm CMOS process. The maximum avalanche gain was 224 for only 8 V bias. The bandwidth was 1.6 GHz for low avalanche gain and 800 MHz for large avalanche gain.

Introduction

Data transmission speed in electronic systems can be enhanced by using optical transmission technique, and the optical transmission has been examined to be applied in board-to-board and chip-to-chip data transmission. In these applications, short wavelength vertical-cavity surface-emitting lasers (VCSELs) and Si photodiodes (PDs) are used for cost-effective applications. Si PDs fabricated by Si CMOS process are expected for monolithic integration with transimpedance amplifiers, limiting amplifiers and following electronic circuits. Fast PDs fabricated by CMOS process using bulk Si have the responsivity of about 0.04 A/W and the bandwidth of about 1 GHz at 850 nm^{1,2}. In these PDs, the photocurrent generated in the substrate is canceled by differential configuration consisting of an illuminated and a shaded PDs. As a result, the bandwidth is increased at the sacrifice of the responsivity. The bandwidth can be easily increased to 10 GHz by using a silicon-on-insulator (SOI) substrate^{3,4}, and the responsivity is, however, 0.08 A/W because of the thin Si layer on the insulator. Recently, avalanche photodiodes (APDs) fabricated by standard CMOS process are reported^{5,6}, and the avalanche gain is, however, less than 5.

Here we report a Si APD fabricated by standard 0.18 μm CMOS process. The APD has the maximum avalanche gain of 250 with 800 MHz bandwidth.

Structure

Figure 1 shows the schematic structure of the APD by standard 0.18 μm CMOS process, which was fabricated in Rohm Corporation in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo. The thickness and the doping concentration of the n-well, the n⁺-layer and the p⁺-layer are not disclosed. The light is illuminated from the top of the APD. When the APD is reverse biased, the n-well is depleted and the photo-generated carriers generated in the n-well is drifted toward the n⁺- and the p⁺-layers, and then extracted as a photocurrent. However, the depth of the n-well in CMOS process is very shallow (typically 1~2 μm), and the most of the illuminated light is penetrated into the p-substrate. The features of our PD are as follows.

1. In conventional CMOS process, silicides are formed on the n⁺- and the p⁺-layers to achieve low contact resistance with metal electrodes. In the CMOS process we utilized, silicides can be

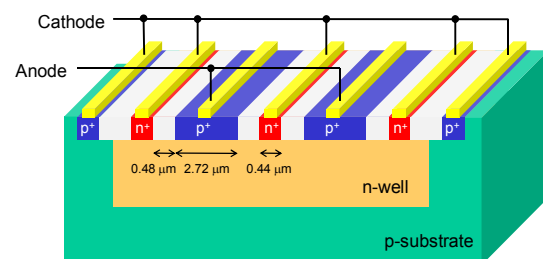


Fig. 1: Schematic structure of the fabricated APD.

formed on a portion of the n⁺- and the p⁺-layers, and then silicide-free n⁺- and the p⁺-layers can be obtained. Since silicides absorb light, the silicide-free region is useful for efficient photo-detection.

2. The n⁺-layers in the n-well and the p⁺-layers outside the n-well are electrically connected to cancel the photo-generated carriers generated in the p-substrate. The photo-generated holes and electrons generated in the p-substrate are collected by the p⁺-layers outside the n-well and the n⁺-layer in the n-well, respectively, and then the holes and the electrons are recombined and are not contributed to the photocurrent.

The silicide widths for the n⁺- and the p⁺-layers are 0.44 μm and 0.72 μm , respectively, which are the minimum width determined by the design rules of the process. Between the n⁺- and the p⁺-layers, 0.48 μm -wide oxide regions are formed for electrical isolation. The widths of the silicide-free p⁺-layers are 2 μm . The detection area is 20 x 20 μm^2 .

Characterization

Figure 2 shows the measured I-V characteristics with and without the optical illumination. The wavelength of the illuminated light is 650 nm. The dark current is about 3 nA, and is drastically increased when the bias is about 8 V; about 9 nA at 8 V bias and more than 1 mA at 8.1 V bias; which means the breakdown voltage is 8.1 V. In silicon pn diodes, when the breakdown voltage is larger than $6E_g/q = 6.7$ V, the breakdown is caused by avalanche mechanism, and then the breakdown of the APD is caused by avalanche mechanism. Under light illumination, the photocurrent is almost constant when the bias is less than 4 V, and is gradually increased, especially when

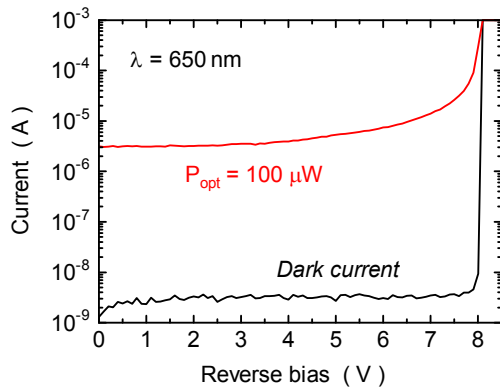


Fig. 2: Measured I-V characteristics. The wavelength of the illuminated light was 650 nm.

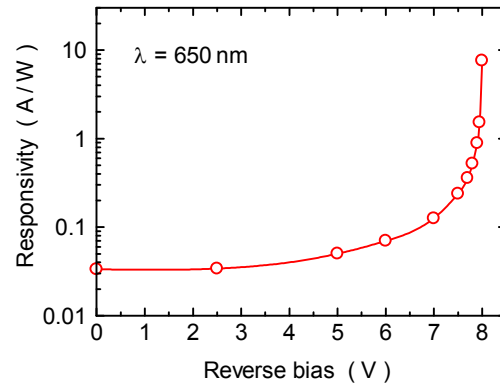


Fig. 3: Measured responsivity against the reverse bias voltage.

the bias is above 6 V. For example, the photocurrent near 8 V bias is about 100 times larger than that at low bias region without increasing the dark current. The extreme current increase is due to avalanche amplification below the p⁺-layers in the n-well.

Figure 3 shows the measured responsivity against the bias voltage at 650 nm wavelength. The responsivity is derived from the photocurrent change against the illuminated optical power below 10 μW to avoid nonlinear photocurrent change. The responsivity in low bias region is 0.034 A/W, which is lower than that of commercial Si photodiodes (typically 0.4 A/W at 650 nm wavelength). One reason is that about 30% of the Si surface is covered by the silicides for electrode forming, and the other is due to the cancellation of photo-generated carriers generated in the p-substrate. The responsivity is increased with the bias voltage, is 7.6 A/W at 8 V bias voltage, showing the avalanche gain be 224. The obtained avalanche gain is the largest gain in Si CMOS APDs reported to date. It is worth noting that the large avalanche gain is obtained even in 8 V voltage, in contrast with the conventional APD (typically 150 V).

Figure 4 shows the measured frequency response of the APD. The measurement bandwidth was about 2 GHz, due to limitation of the laser source. When the bias is less than 7.9 V, the 3 dB bandwidth is almost unchanged and is 1.6 GHz. The 3 dB bandwidth at 8.0 V bias voltage is decreased to 800 MHz, which is due to multiplication time in avalanche amplification occurred in large avalanche gain.

Conclusions

In conclusion, a Si APD is fabricated by standard 0.18 μm CMOS process, and is characterized. The APD has interdigital electrode structure, and the silicide-free p⁺-layers are used for efficient optical absorption. At 650 nm wavelength, the responsivity is 0.034 A/W in low bias region, and is increased to 7.6 A/W at only 8 V bias voltage due to avalanche

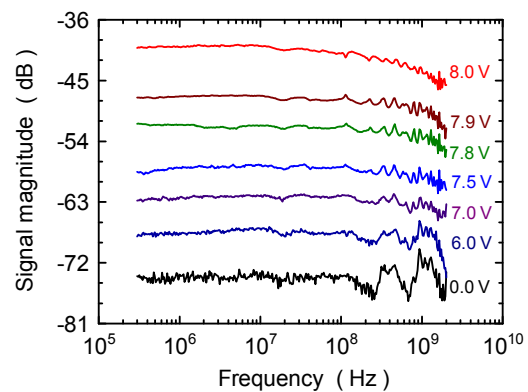


Fig. 4: Measured frequency response for various reverse bias voltage.

amplification, and the resultant maximum avalanche gain was 224. The bandwidth was 1.6 GHz at low bias region and 800 MHz for large avalanche region.

Acknowledgement

The APD has been fabricated in the chip fabrication program of VLSI Design and Education Center (VDEC), the University of Tokyo, in collaboration with Rohm Corporation and Toppan Printing Corporation.

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