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#### Abstract

We discuss the stability of an adiabatic stepwise-charging circuit with advanced series capacitors, which is effective for the reduction of the applied voltage to each capacitor. SPICE simulation shows that this circuit is stable even if the initial voltages are lower than zero. For the analytical discussion, we derive a matrix that connects charge and voltage in the circuit and show that the matrix is a positive-definite symmetric one. Therefore, the step voltage is generated spontaneously. We also derive energy dissipation analytically using tank capacitor voltage. Using this formula and SPICE simulation, we clarify that energy dissipation decreases monotonically as a function of time and finally reaches the minimum value.


Keywords: adiabatic charging, charge recycling, series capacitors, a positive-definite symmetric matrix, stability, energy dissipation
Classification: Integrated circuits

## References

[1] L. J. Svensson and J. G. Koller, "Driving a capacitive load without dissipating $f C V^{2}$," Proc. IEEE Symp. Low Power Electron., pp. 100-101, 1994.
[2] R. Lal, W. Athas, and L. Svensson, "A low power adiabatic driver system for AMLCDs," Proc. IEEE Symp. VLSI Circuits, pp. 198-201, 2000.
[3] S. Nakata, "Stability of adiabatic circuit using asymmetric 1D-capacitor array between the power supply and ground," IEICE Electron. Express, vol. 4, no. 5, pp. 165-171, 2007.
[4] M. van Elzakker et al., "A $1.9 \mu \mathrm{~W} 4.4 \mathrm{fJ} /$ conversion-step $10 \mathrm{~b} 1 \mathrm{MS} / \mathrm{s}$ Charge-Redistribution ADC," Proc. ISSCC Dig., pp. 244-245, 2008.
[5] S. Nakata, T. Kusumoto, M. Miyama, and Y. Matsuda, "Adiabatic SRAM
with a Large Margin of $\mathrm{V}_{\mathrm{T}}$ Variation by Controlling the Cell-Power-Line and Word-Line Voltage," Proc. IEEE ISCAS, pp. 393-396, 2009.
[6] S. Nakata, Y. Katagiri, and S. Matsuno, "Electrostatic energy, potential energy and energy dissipation for a width-variable capacitor system during adiabatic charging," J. Appl. Phys., vol. 101, p. 034911, 2007.

## 1 Introduction

Reducing the power dissipation of circuits is an important issue. A charge recycling regenerator with a switched capacitor circuit is one of the most promising solutions and has been researched for adiabatic logic [1, 2, 3, 4]. In a previous article [5], we proposed a switched capacitor circuit with advanced series capacitors and showed by SPICE that the tank capacitor voltage converges to the step voltage spontaneously when the initial voltages are larger than or equal to zero. However, it is not clear whether the circuit is stable when they are negative (i.e., below the value of GND), which is often caused by external noise.

In this article, we confirm by SPICE that the circuit is stable even if the initial voltages are negative and that the circuit reaches the stable state five times as rapidly as the conventional one [1]. The stability of this circuit is proved generally by an analytical method. We also discuss the energy dissipation as a function of time. It is clarified that, although the voltages of the tank capacitor change variously (sometimes increase and sometimes decrease), the energy dissipation always decreases monotonically and finally reaches the minimum value.

## 2 Stability of the regenerator with series capacitors

The conventional switched capacitor regenerator circuit and the regenerator with the advanced series capacitors are shown in Figs. 1 (a) and (b). This series capacitors circuit is advanced compared to the previous series one [3] because, in the four-step case, the number of tank capacitors $C_{i}$ decreases from 4 to 3 , which is the same as in Fig. 1 (a). Therefore, we can reduce


Fig. 1. Switched capacitor circuit. (a) Conventional circuit. (b) Advanced series capacitors circuit.
the number of capacitors by using the advanced one. In Figs. 1 (a) and (b), $C_{L}$ is load capacitance, $V$ is the power supply voltage, $V_{\text {out }}$ is output voltage, and $V_{C i}$ is the voltage of the node connected to the upper plate of $C_{i}$. The switching transistor is a parallel connection of pMOSFETs and nMOSFETs. T0, T1, T2, T3, T4, T3, T2, and T1 turn on successively and this operation is repeated.

The circuit simulation results are shown in Fig. 2. We used the $0.25-\mu \mathrm{m}$ design rule. Threshold voltages were 0.4 and -0.4 V in the nMOS and pMOS transistors, respectively. $C_{1}, C_{2}$, and $C_{3}$ were the same value: $100 \mathrm{pF} . C_{L}$ was 0.4 pF . The period of the four-step waveform cycle was $0.2 \mu \mathrm{~s}$. The initial $V_{C 1}, V_{C 2}$, and $V_{C 3}$ values were set to -0.4 V . The gate width was $6 \mu \mathrm{~m}$. The gate length and $V$ are $0.25 \mu \mathrm{~m}$ and 2 V in Fig. 2 (a), and $0.5 \mu \mathrm{~m}$ and 4 V in Fig. 2 (b), respectively. In Fig. 2, the blue and red lines show the advanced series circuit and the conventional one, respectively. In both cases, after $200 \mu \mathrm{~s}, V_{C i}$ becomes $i V / 4$ spontaneously. From the results, it is clear that the advanced series circuit is very stable even if the initial $V_{C i}$ is negative due to external noise and that it reaches the stable state five times as rapidly as the conventional one. Another feature of the advanced series circuit is that the voltage of the capacitors is smaller than $V / 4$ due to the series connection. On the other hand, for the conventional one, the maximum voltage of the capacitors is $3 \mathrm{~V} / 4$. This difference is a serious problem when we use an electric double layer capacitor (EDLC). The endurance voltage of the EDLC is 2.5 V so that we cannot use the conventional circuit with $V=4 \mathrm{~V}$ because $V_{C 3}$ in Fig. 1 (a) reaches 3 V as shown in Fig. 2 (b).


Fig. 2. Voltage change of $V_{C i}$ when $V$ is (a) 2 and (b) 4 V . The blue and red lines are for the advanced series circuit and conventional one, respectively.

Next, we investigate the reason for the stability generally by using an analytical method. Here, we assume that $C_{i} \gg C_{L}$. The $y_{i}$ is the node connected to the upper plate of $C_{i}$. Let $Q_{t i}$ be the transferred charge quantity from $y_{i}$ to $C_{L}$ at the $i$ th step voltage [Fig. 3 (a)] and $Q_{r i}$ be the restored charge from $C_{L}$ to $y_{i}$ [Fig. $\left.3(\mathrm{~b})\right]$. We define $Q_{i}$ as the amount of charge stored in the capacitor plates connected to $y_{i}$. Then, assuming that the number of the steps is $N, V_{C 0}=0$, and $V_{C N}=V, \Delta Q_{i}$ (the change of $Q_{i}$ ) after charging
and restoring can be written as [3]

$$
\begin{equation*}
\Delta Q_{i}=-Q_{t i}+Q_{r i}=C_{L}\left(V_{C(i-1)}-2 V_{C i}+V_{C(i+1)}\right), \quad(1 \leq i \leq N-1) \tag{1}
\end{equation*}
$$

Here, we define $V_{i}$ as $V_{i}=V_{C i}-i V / N$. Using $V_{i}$ and (1), we have

$$
\begin{equation*}
\Delta Q_{i}=C_{L}\left(V_{i-1}-2 V_{i}+V_{i+1}\right), \quad(1 \leq i \leq N-1) \tag{2}
\end{equation*}
$$

Next, we define $v_{i}$ as the voltage difference between the capacitor plates [Fig. 3 (a)]. Then, using $V_{C i}=v_{1}+v_{2}+\cdots+v_{i-1}+v_{i}$, we have

$$
\left[\begin{array}{c}
V_{C 1}  \tag{3}\\
\vdots \\
V_{C(N-1)}
\end{array}\right]=\boldsymbol{B}\left[\begin{array}{c}
v_{1} \\
\vdots \\
v_{N-1}
\end{array}\right], \text { where } \boldsymbol{B}=\left[\begin{array}{ccc}
1 & & 0 \\
\vdots & \ddots & \\
1 & \cdots & 1
\end{array}\right]
$$




Fig. 3. Definitions of charge and voltage in the regenerator. (a) $Q_{t i}$ is transferred from $y_{i}$ to $C_{L}$ at the $i$ th step. (b) $Q_{r i}$ is restored from $C_{L}$ to $y_{i}$ at the $i$ th step.

From Fig. 3, we have

$$
\left[\begin{array}{c}
Q_{1}  \tag{4}\\
Q_{2} \\
\vdots \\
Q_{N-1}
\end{array}\right]=\boldsymbol{D}\left[\begin{array}{c}
v_{1} \\
v_{2} \\
\vdots \\
v_{N-1}
\end{array}\right], \text { where } \boldsymbol{D}=\left[\begin{array}{ccccc}
C_{1} & -C_{2} & & & 0 \\
& C_{2} & -C_{3} & & \\
& & \ddots & \ddots & \\
& & & C_{N-2} & -C_{N-1} \\
0 & & & & C_{N-1}
\end{array}\right]
$$

Then, using (3) and (4), and considering the difference in $Q_{i}$ and $V_{C i}$ after one cycle operation, we have

$$
\left[\begin{array}{c}
\Delta Q_{1}  \tag{5}\\
\vdots \\
\Delta Q_{N-1}
\end{array}\right]=\boldsymbol{D} \boldsymbol{B}^{-1}\left[\begin{array}{c}
\Delta V_{C 1} \\
\vdots \\
\Delta V_{C(N-1)}
\end{array}\right]
$$

where $\Delta V_{C i}$ is the change of $V_{C i}$ after charging and restoring. Using (5) and $\Delta V_{C i}=\Delta V_{i}$, we have

$$
\left[\begin{array}{c}
\Delta Q_{1}  \tag{6}\\
\vdots \\
\Delta Q_{N-1}
\end{array}\right]=\boldsymbol{F} \cdot\left[\begin{array}{c}
\Delta V_{1} \\
\vdots \\
\Delta V_{N-1}
\end{array}\right], \text { where } \boldsymbol{F}=\boldsymbol{D} \boldsymbol{B}^{-1}
$$

The $\boldsymbol{B}^{-1}$ is calculated as in ref. 3. Therefore, we have

$$
\boldsymbol{F}=\boldsymbol{D} \boldsymbol{B}^{-1}=\left[\begin{array}{ccccc}
C_{1}+C_{2} & -C_{2} & & &  \tag{7}\\
-C_{2} & C_{2}+C_{3} & -C_{3} & & \\
& -C_{3} & \ddots & \ddots & \\
& & \ddots & C_{N-2}+C_{N-1} & -C_{N-1} \\
& & & -C_{N-1} & C_{N-1}
\end{array}\right]
$$

Using (7), we have

$$
\begin{equation*}
\boldsymbol{x}^{t} \boldsymbol{F} \boldsymbol{x}=C_{1} x_{1}^{2}+C_{2}\left(x_{1}-x_{2}\right)^{2}+\cdots+C_{N-1}\left(x_{N-2}-x_{N-1}\right)^{2} \tag{8}
\end{equation*}
$$

where $\boldsymbol{x}$ is one of any vector. While the $\boldsymbol{F}$ is different from that in ref. 3, we easily find that it is a positive-definite symmetric matrix so that step voltage is generated spontaneously using the theory in ref. 3 .

## 3 Time variation of energy dissipation

Next, we investigate how the energy dissipation changes as a function of time. In the four-step case, the work done by the regenerator during charging $W_{1}$ is written as [6]
$W_{1}=V_{C 1} \Delta Q_{1}+V_{C 2} \Delta Q_{2}+V_{C 3} \Delta Q_{3}+V_{C 4} \Delta Q_{4}$
$=C_{L}\left[V_{C 1} V_{C 1}+V_{C 2}\left(V_{C 2}-V_{C 1}\right)+V_{C 3}\left(V_{C 3}-V_{C 2}\right)+V_{C 4}\left(V_{C 4}-V_{C 3}\right)\right]$.
The work done by the regenerator when restoring $W_{2}$ is written as

$$
\begin{align*}
& W_{2}=-V_{C 1} \Delta Q_{2}-V_{C 2} \Delta Q_{3}-V_{C 3} \Delta Q_{4} \\
& =-C_{L}\left[V_{C 1}\left(V_{C 2}-V_{C 1}\right)+V_{C 2}\left(V_{C 3}-V_{C 2}\right)+V_{C 3}\left(V_{C 4}-V_{C 3}\right)\right] \tag{10}
\end{align*}
$$

$W_{2}$ is negative, which means the regenerator gets energy from $C_{L}$. Using the energy conservation law, we have

$$
\begin{equation*}
W_{1}=E_{d i s s 1}+U \tag{11}
\end{equation*}
$$

where $E_{d i s s 1}$ is the energy dissipation during charging and $U$ is the electrostatic energy of a load capacitor. We also have

$$
\begin{equation*}
U=-W_{2}+E_{d i s s 2} \tag{12}
\end{equation*}
$$

where $E_{d i s s 2}$ is the energy dissipation during restoring. Therefore, using (11) and (12), we have

$$
\begin{equation*}
W_{1}+W_{2}=E_{d i s s 1}+E_{d i s s 2}=E_{d i s s} \tag{13}
\end{equation*}
$$

where $E_{\text {diss }}$ is the total energy dissipation during one cycle. Then, using (9) and (10), we have

$$
\begin{equation*}
E_{\text {diss }}=C_{L}\left[V_{C 1}^{2}+\left(V_{C 2}-V_{C 1}\right)^{2}+\left(V_{C 3}-V_{C 2}\right)^{2}+\left(V_{C 4}-V_{C 3}\right)^{2}\right] . \tag{14}
\end{equation*}
$$

The minimum of $E_{\text {diss }}$ is calculated using the method of Lagrange multipliers. We denote $q_{1}, q_{2}, q_{3}$, and $q_{4}$ as

$$
\begin{equation*}
q_{1}=V_{C 1}, q_{2}=V_{C 2}-V_{C 1}, q_{3}=V_{C 3}-V_{C 2}, q_{4}=V_{C 4}-V_{C 3} \tag{15}
\end{equation*}
$$

Then, we have $q_{1}+q_{2}+q_{3}+q_{4}=V$. We define $L$ as

$$
\begin{equation*}
L=E_{d i s s}-\lambda\left(q_{1}+q_{2}+q_{3}+q_{4}-V\right) \tag{16}
\end{equation*}
$$

By calculating $\partial L / \partial q_{i}=0$ and $\partial L / \partial \lambda=0$, we have $q_{1}=q_{2}=q_{3}=q_{4}$ easily, which means $V_{C i}=i V / 4$. Therefore, it is clarified that $E_{\text {diss }}$ takes the minimum when the step voltage is generated. Regarding the time variation of $E_{\text {diss }}$, we can calculate this value using SPICE.

The simulation result is shown in Fig. 4 (a). The lower lines show $E_{\text {diss }}$ of the advanced series circuit (blue) and the conventional one (red) with the condition in Fig. 2 (a). The upper ones show those with almost the same condition but with $V_{C 1}=2.4, V_{C 2}=-0.4, V_{C 3}=1.0 \mathrm{~V}$, and $C_{1}, C_{2}$, and $C_{3}$ values of 100,50 , and 100 pF , respectively. First, we discuss the lower lines. When $t=0 \mathrm{~s}, E_{\text {diss }} / C_{L}$ is equal to 5.9 , which is valid from the initial condition. When $t=200 \mu \mathrm{~s}, E_{\text {diss }} / C_{L}$ is equal to 1 , which is also valid from the final state such that $V_{C i}=i V / 4$. The $E_{\text {diss }}$ in the advanced series circuit decreases more rapidly than in the conventional one. This means that the circuit reaches the stable state more rapidly than the conventional one.

Next, we consider the upper lines. The change of $V_{C i}$ with this condition is shown in Fig. 4 (b). The blue and red lines in Fig. 4 (b) are $V_{C i}$ of the advanced series circuit and the conventional one, respectively. In the upper lines in Fig. 4 (a), $E_{\text {diss }}$ in the conventional circuit (red) decreases more rapidly than in the advanced series one (blue) at this time. However, this initial $V_{C i}$ is a very rare case and would hardly ever occur. Normally, the initial $V_{C i}$ is around zero as in Fig. 2 (a), at which we can easily confirm that $E_{\text {diss }}$ in the


Fig. 4. (a) Time variation of energy dissipation during one cycle in the circuit with advanced series capacitors (blue) and with the conventional ones (red).
(b) Change of $V_{C i}$ in the advanced series circuit (blue) and the conventional one (red) when the initial $V_{C 1}, V_{C 2}$, and $V_{C 3}$ are $2.4,-0.4$, and 1.0 V , respectively.
advanced series circuit decreases more rapidly than that in the conventional one. This means the stable state in the advanced series circuit is generated more rapidly. We can say that this is the merit of the advanced series circuit.

Regarding the time variation of $E_{\text {diss }}$, interestingly, $E_{\text {diss }}$ in both circuits decreases monotonically and reaches the minimum value, even if the voltages change variously as in Fig. 4 (b). This means, in other words, that the voltage state in the circuit proceeds in a direction such that the energy dissipation becomes smaller and finally reaches the minimum value. This phenomenon in the circuit reminds us of the other principle in the electromagnetic theory; namely, that the steady-state current distribution in a conductor always satisfies the condition such that the energy dissipation (Joule energy) is the minimum value.

## 4 Conclusion

In summary, we analyzed an adiabatic circuit with advanced series capacitors. We confirmed by SPICE that this circuit is stable even if the initial voltages are negative and proved its stability generally by an analytical method. We also clarified that the voltage state in the circuit proceeds in a direction such that the energy dissipation becomes smaller and finally reaches the minimum value.

