

Improvement of charge trapping characteristics of Al₂O₃/Al-rich Al₂O₃/SiO₂ stacked films by thermal annealing

メタデータ	言語: eng 出版者: 公開日: 2017-10-03 キーワード (Ja): キーワード (En): 作成者: メールアドレス: 所属:
URL	https://doi.org/10.24517/00009024

This work is licensed under a Creative Commons Attribution-NonCommercial-ShareAlike 3.0 International License.



Improvement of Charge Trapping Characteristics of Al₂O₃/Al-rich Al₂O₃/SiO₂ Stacked Films by Thermal Annealing

Shunji Nakata ^{a, *}, Takashi Kato ^b, Shinya Ozaki ^b, Takeshi Kawae ^b, and
Akiharu Morimoto ^{b, **}

^aNTT Microsystem Integration Laboratories, Atsugi 243-0198, Japan

^bGraduate School of Natural Science and Technology, Kanazawa University,
Kanazawa 920-1192, Japan

^{*})Electronic mail: nakata.shunji@lab.ntt.co.jp

^{**})Electronic mail: amorimot@ec.t.kanazawa-u.ac.jp

Thin film Al₂O₃/Al-rich Al₂O₃/SiO₂ structures were fabricated on p-Si substrates. Radio-frequency magnetron co-sputtering was used to form Al-rich Al₂O₃ thin film as the charge-trapping layer of nonvolatile Al₂O₃ memory. Capacitance-voltage measurements showed a large hysteresis due to charge trapping in the Al-rich Al₂O₃ layer. The charge trap density was estimated to be $42.7 \times 10^{18} \text{ cm}^{-3}$, which is the largest value ever reported for an Al-rich Al₂O₃ layer; it is six times larger than that of a conventional metal-nitride-oxide-silicon memory. Thermal annealing was found to reduce the leakage current of the Al₂O₃ blocking layer, thereby providing this structure with better data retention at room temperature than an as-deposited one. In addition, the annealed structure was found to exhibit good data retention even at 100°C.

Key words: Radio-frequency magnetron sputtering, Oxides, Al-rich Al₂O₃, SiO₂, Charge trapping, C-V hysteresis, Thermal annealing

1. Introduction

Nonvolatile semiconductor memory devices are being widely studied because of their low-power operation, high memory density per volume, and other attractive features. Charge trap memories [1-7] are a subject of special interest for nanoscale devices [8-11] because their simple structure should enable extremely large-scale integration.

Recently, we fabricated a simple trap memory consisting of a SiO₂ tunnelling insulator, an Al-rich Al₂O₃ charge trapping layer, and an Al₂O₃ blocking insulator [12]. The capacitance-voltage (C-V) characteristics exhibit a large hysteresis. This is a promising structure because the layer on the tunnelling insulator contains only two elements (Al, O). Although this simple gate structure is suitable for a low-cost memory, there are a couple of problems with it. One is that there are large defects in the Al₂O₃ blocking layer because the sample was not annealed after deposition. Another problem is that the use of a low-resistivity wafer ($\rho \cong 1.5 \times 10^{-2} \Omega \text{ cm}$) makes the width of the semiconductor depletion layer, W , small. This makes the capacitance, C_D , of the semiconductor depletion layer large, which results in a large minimum capacitance, C_{min} , in the C-V curve, where C_{min} equals the series capacitance of C_D and the gate insulator capacitance, C_i . In consequence, there is a small difference between the capacitance after writing and that after erasing, which is not suitable for capacitance measurements. One more problem is that the sample was made on an n-Si wafer, for which the carriers are holes and the mobility is low.

In this study, we fabricated an Al₂O₃/Al-rich Al₂O₃/SiO₂ structure on a p-Si substrate with a high resistivity ($\rho \cong 1 \Omega \text{ cm}$) to obtain a smaller C_{min} and thus a larger difference between the capacitance after writing and that after erasing. Moreover, the use of a p-Si substrate, for which the carriers are electrons, also provides a higher

mobility. We used this structure to investigate the effects of annealing by comparing the C-V characteristics of as-deposited and annealed samples. We also investigated data retention by measuring the timewise change in capacitance at room temperature and at 100°C.

2. Experiments

2.1. Film deposition

Radio-frequency (RF) magnetron co-sputtering was used to form Al-rich Al₂O₃ [13]. Al metal plates were placed on an Al₂O₃ target, and the Al content of the Al-O film was controlled by means of the areal ratio of the Al on the target.

Sputtering was carried out with Ar gas at a flow rate of 2 sccm, a pressure of 0.267 Pa, an RF power of 100 W, and an RF frequency of 13.56 MHz. The thickness of deposited film was measured with a spectroscopic ellipsometer. The Al content of the Al-O film was investigated with an electron probe micro-analyzer.

The samples were made on (100) p-Si substrates. First [Fig. 1(a)], the wafers were cleaned with HF for 40 s, and thermal oxidation formed a layer of SiO₂ as a tunnel barrier insulator. The oxidation was carried out in a gas mixture (N₂:O₂ = 3:1) at a temperature of 1000°C for a period of 180 s. It resulted in a 3.4-nm-thick layer of SiO₂.

Next, a 5-nm-thick layer of Al-rich Al₂O₃ as a charge storage layer was deposited by co-sputtering. The Al content was as high as 50%, which is larger than the 40% for stoichiometric Al₂O₃. Then, RF sputtering deposited a 6-nm-thick layer of stoichiometric Al₂O₃ as a blocking barrier insulator. After deposition, the samples were annealed in N₂ gas. The annealing process employed a linear temperature ramp to 400°C in 1 h, followed by a 10-m hold, and a linear cool-down for 3 h. Finally, a

square gate electrode with a width of 50 μm was formed by the thermal evaporation of Al at a pressure of 1.33×10^{-4} Pa. In the band diagram of this structure [Fig. 1(b)], the height of the Al₂O₃ conduction barrier is 2.8 eV with respect to the Si conduction band [14, 15] and 4 eV with respect to the Al Fermi level [16]. In contrast, the height of an HfO₂ conduction barrier is only 1.5 eV with respect to the Si conduction band [15]. So, the barrier height is larger for Al₂O₃/Si than for HfO₂/Si. This high barrier is better at trapping carriers, which makes it more suitable for making nonvolatile memory. The role of the localized energy level due to Al-rich AlO is to trap a carrier in the level or release it from the level.

2.2. Capacitance-voltage characteristics

We measured the high-frequency C-V characteristics of as-deposited and annealed Al-rich Al₂O₃ structures with an Al content of 50%. The measurements were performed at a frequency of 1 MHz at room temperature. The p-Si wafer was connected to the ground. The maximum applied gate voltage was 4, 5, 6, or 7 V. When the maximum applied gate voltage was 4 V, the voltage to the gate electrode was swept from 4 V down to -4 V and then back up. The sweep rate was about 1 V/sec. The C-V curves for as-deposited [Fig 2(a)] and annealed [Fig. 2(b)] samples show a large hysteresis due to charge trapping in the Al-rich Al₂O₃ layer. The large hysteresis for the annealed sample shows that the Al-rich Al₂O₃ structure is stable after annealing at a high temperature, such as 400°C. Moreover, the hysteresis curve for the annealed sample does not show any deviations from the ideal one and is almost the same as the ideal one, while that for the as-deposited sample shows deviations. This strongly suggests annealing reduces the number of defects in the

Al₂O₃ blocking layer. The types of defects that cause the deviation are not well understood yet, and further research is necessary to clarify their origin.

Next, we examined whether or not the measured capacitance agreed with the theoretical one calculated from metal-insulator-semiconductor theory. This is very important for determining the electrical field across each layer. The insulator capacitance, C_i , was estimated to be about 10 pF from Figs. 2(a) and (b). It is equal to the series capacitances of the SiO₂, Al-rich Al₂O₃, and Al₂O₃; thus, $1/C_i = 1/C_{SiO_2} + 1/C_{Al-O} + 1/C_{Al_2O_3}$. From the dielectric constant of SiO₂ (3.9), we estimated C_{SiO_2} to be $3.9 \times \epsilon_0 S / 3.4 \text{ nm}$, where ϵ_0 is the vacuum permittivity and S is the sample area. Assuming that $\epsilon_0 = 8.85 \times 10^{-12} \text{ F/m}$ and $S = 2500 \mu\text{m}^2$ yields $C_{SiO_2} = 25.4 \text{ pF}$. Now, the dielectric constant of Al-rich Al₂O₃ with an Al content of 50% is 8.2, which is almost the same as the value of 8.1 for Al₂O₃ [12]. So, to simplify the calculations, we set the dielectric constant of both materials to 8. Recent experimental results have confirmed this value [17]. Using this dielectric constant, C_{Al-O} and $C_{Al_2O_3}$ were estimated to be 35.4 and 29.5 pF, respectively. These values yield an insulator capacitance, C_i , of 9.9 pF, which agrees well with the measured value of 10 pF.

Next, let us consider C_{min} , which is the value when $V = 7 \text{ V}$ in Fig. 2. As previously mentioned, C_{min} is the series capacitance of C_i and the capacitance of the semiconductor depletion layer, C_D : $1/C_{min} = 1/C_i + 1/C_D$. C_D is given by $C_D = \epsilon_{Si} S / W$, where ϵ_{Si} is the permittivity of Si, and W is the width of the semiconductor depletion layer. The formula for W is [18]

$$W^2 = \frac{4\epsilon_{Si} kT}{q^2 N_A} \ln\left(\frac{N_A}{n_i}\right), \quad (1)$$

where k is the Boltzmann constant, q is the elementary charge, N_A is the impurity concentration, and n_i is the intrinsic carrier density. From the resistivity of the p-Si wafer, we estimated N_A to be $1.3 \times 10^{16} \text{ cm}^{-3}$ [18]. Thus, assuming that $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$ yields $\ln(N_A / n_i) = 13.7$. If we further assume that $T = 293 \text{ K}$ and $\varepsilon_{Si} = 11.9 \times 8.85 \times 10^{-12} \text{ F/m}$, the width, W , is 265 nm. Thus, $C_D = \varepsilon_{Si} S / W = 1.0 \text{ pF}$. Using the values obtained for C_i and C_D , we have $C_{min} = 0.9 \text{ pF}$, which agrees well with the measured value (1 pF).

Now, let us consider the hysteresis voltage window, ΔV , as a function of the maximum applied gate voltage (Fig. 3). ΔV is the voltage difference at the midpoint between the high and the low capacitance. The blue symbols show ΔV as a function of the maximum applied gate voltage calculated from Fig. 2(b). The red ones show how ΔV changes as the maximum applied gate voltage varies from 4 to 12 V. ΔV reaches 8.2 V at a gate voltage of 12 V. This means that a large applied gate voltage causes a large number of charges to be trapped in the Al-rich Al₂O₃ layer.

2.3. Charge trap density

We examined the charge trap density of annealed Al-rich Al₂O₃ film so that we could compare it to that of metal nitride-oxide silicon (MNOS) ($7 \times 10^{18} \text{ cm}^{-3}$) [19]. The stored charge per unit area, ΔQ , is given by $\Delta Q = C_b \Delta V / 2$ [19], where C_b is the capacitance per unit area of the blocking barrier insulator and ΔV is the hysteresis voltage window discussed above. C_b is given by $C_b = \varepsilon / d_b$, where d_b is the thickness of the blocking insulator and ε is its permittivity. d_b is the distance between the gate and the center of the charge storage layer: $d_b = 6 + 5/2 = 8.5 \text{ nm}$; and ε is $8 \times 8.85 \times 10^{-12} \text{ F/m}$. These values yield a C_b of about $8.33 \times 10^{-3} \text{ F/m}^2$. Since ΔV is

8.2 V when the applied gate voltage is 12 V (Fig. 3), ΔQ for an Al-rich Al₂O₃ memory is 34.2×10^{-7} C/cm². As a result, the estimated electron trap density, $N_e = \Delta Q / (5 \text{ nm} \times 1.6 \times 10^{-19} \text{ C})$, is 42.7×10^{18} cm⁻³. This value is six times larger than that for MNOS [19]. Furthermore, to our knowledge, it is the largest value ever reported for an Al-rich Al₂O₃ memory. Table I compares the sheet carrier density, n_s , of various samples. In this study, n_s was found to be 42.7×10^{18} cm⁻³ $\times 5$ nm = 2.14×10^{13} cm⁻², which is the largest value ever reported. A large n_s is suitable for trapping charges in the charge storage layer and is desirable for nanoscale devices in which the number of trap sites is insufficient due to statistical fluctuations, as is the case for MNOS.

2.4. Data Retention

The final topic is data retention. To measure the change in capacitance for as-deposited [Fig. 4(a)] and annealed [Fig. 4(b)] samples, we first applied a voltage of 7 V to the gate for 1 s and measured the change in capacitance over time at a gate voltage of 0 V. The initial capacitance was about 9 pF (State A in Fig. 4). Next, we applied a voltage of -7 V to the gate for 1 s and measured it again over time at a gate voltage of 0 V. In this case, the initial capacitance was 1 pF (State B in Fig. 4). The black symbols in Fig. 4 indicate measurement results for room temperature, and the red symbols in Fig. 4(b) indicate results for a temperature of 100°C.

For the as-deposited sample, the large capacitance [A in Fig. 4(a)] drops to 30% after 10⁴ s; but for the annealed sample, the capacitance [A in Fig. 4(b)] remains as large as 90% after 10⁴ s at both room temperature and 100°C. This means that the device should be able to store data for more than 3 $\times 10^8$ s. The reason for the good

data retention is that thermal annealing reduces the leakage current of the Al₂O₃ blocking layer.

There are two more points regarding Fig. 4(b). One is that the capacitance for B does not change as much as that for A. This is because the initial capacitance for A is located on a steep part of the slope of the C-V curve [Fig. 2(b)], while that for B is located on more gradual slope. The flat-band voltage shift changes in proportion to $\log t$. So, the change in capacitance depends on the initial position on the C-V curve.

The other point is that the initial capacitance at a temperature of 100°C is lower than that at room temperature. This is probably because the initial flat-band voltage shift is smaller at 100°C than at room temperature, which might be caused by carrier detrapping at a high temperature. These two points become much clearer in the following discussion of the flat-band voltage shift.

Here, we investigate flat-band voltage shift as a function of time. It changes in proportion to $\log t$. First, the flat-band capacitance, C_{FB} , in Fig. 2(b) is given by [18]

$$C_{FB} = \frac{1}{1/C_i + L_D/(\epsilon_{Si}S)}, \text{ where } L_D = \sqrt{\frac{kT\epsilon_{Si}}{N_A q^2}}. \quad (2)$$

The L_D obtained from N_A is $L_D = 3.58 \times 10^{-8}$ m. Thus, we have

$$\frac{\epsilon_{Si}S}{L_D} = \frac{11.9 \times 8.85 \times 10^{-12} \text{ F/m} (50 \times 10^{-6} \text{ m})^2}{35.8 \text{ nm}} = 7.35 \times 10^{-12} \text{ F} \quad (3)$$

and

$$\begin{aligned} C_{FB} &= \frac{1}{1/C_{Al_2O_3} + 1/C_{AlO} + 1/C_{SiO_2} + L_D/(\epsilon_{Si}S)} \\ &= \frac{1}{1/9.9 \text{ pF} + 1/7.35 \text{ pF}} = 4.2 \text{ pF}. \end{aligned} \quad (4)$$

Using this C_{FB} , we calculated the flat-band voltage shifts to be 1.66 and -1.68 V from the right- and leftmost C-V curves in Fig. 2(b), respectively.

Next, from the change in capacitance in Fig. 4(b), we calculated the flat-band voltage shift as a function of time. We assumed that the rightmost C-V curve in Fig. 2(b) did not change shape and just moved to the left as t increased. Similarly, we assumed that the leftmost curve did not change shape and just moved to the right as t increased. The flat-band voltage shift over time (Fig. 5) can be calculated from the change in capacitance. The flat-band voltage shift changes in proportion to $\log t$. The solid lines are extrapolations. This graph indicates that this device should be able to store data for more than 10 years.

3. Conclusion

In summary, we deposited Al₂O₃/Al-rich Al₂O₃/SiO₂ thin films on p-Si substrates by RF magnetron co-sputtering. From C-V hysteresis measurements, we found that this structure provides the largest charge trap density ever reported for Al-rich Al₂O₃; the value is six times larger than that for MNOS. The results of a data retention experiment indicate that the device should be able to store data for almost ten years. The simple structure of the gate makes this a promising structure for low-cost nonvolatile memory.

References

- [1] F. R. Libsch and M. H. White, *Solid State Electron.*, 33 (1990) 105.
- [2] C.H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park and K. Kim, *Tech. Dig. Int. Electron Devices Meet.*, 2003, pp. 613.
- [3] Y.N. Tan, W. K. Chim, W. K. Choi, M. S. Joo, T. H. Ng, and B. J. Cho, *Tech. Dig. Int. Electron Devices Meet.*, 2004, pp. 889.
- [4] M. Specht, H. Reisinger, F. Hofmann, T. Schulz, E. Landgraf, R. J. Luyken, W. Rösner, M. Grieb, and L. Risch, *Solid State Electron.*, 49 (2005) 716.
- [5] S. Nakata, K. Saito, and M. Shimada, *Appl. Phys. Lett.* 87 (2005) 223110.
- [6] S. Nakata, K. Saito, and M. Shimada, *Jpn. J. Appl. Phys.* 45 (2006) 3176.
- [7] W. Cho, S. S. Lee, T. -M. Chung, C. G. Kim, K. -S. An, J. -P. Ahn, J. -Y. Lee, J. -W. Lee, and J. -H. Hwang, *Electrochemical and Solid-State Lett.* 13 (2010) H209.
- [8] *Single Charge Tunneling*, edited by H. Grabert and M. H. Devoret (Plenum, New York, 1992).
- [9] S. Nakata, *Phys. Rev. B* 47 (1993) 1679.
- [10] P. D. Dresselhaus, L. Ji, Siyuan Han, J. E. Lukens, and K. K. Likharev, *Phys. Rev. Lett.* 72 (1994) 3226.
- [11] N. J. Stone and H. Ahmed, *Appl. Phys. Lett.* 73 (1998) 2134.
- [12] S. Nakata, R. Maeda, T. Kawae, A. Morimoto, and T. Shimizu, *Thin Solid Films* 520 (2011) 1091.
- [13] S. Nakata, S. Nagai, M. Kumeda, T. Kawae, A. Morimoto, and T. Shimizu, *J. Vac. Sci. Technol. B* 26 (2008) 1373.
- [14] J. Robertson, *J. Vac. Sci. Technol. B* 18 (2000) 1785.

- [15] T. Sugizaki, M. Kobayashi, M. Ishidao, H. Minakata, M. Yamaguchi, Y. Tamura, Y. Sugiyama, T. Nakanishi, and H. Tanaka, Symposium on VLSI Technology, 2003, pp. 27.
- [16] T. M. Pan and F. H. Chen, Semicond. Sci. Technol. 26 (2011) 045004.
- [17] B. Lee, G. Mordi, M. J. Kim, Y. J. Chabal, E. M. Vogel, R. M. Wallace, K. J. Cho, L. Colombo, and J. Kim, Appl. Phys. Lett. 97 (2010) 043107.
- [18] S. M. Sze, Physics of Semiconductor Devices, second edition, John Wiley and Sons, New York, 1981.
- [19] S. Minami, and Y. Kamigaki, IEEE Trans. Electron Devices, ED-38 (1991) 2519.
- [20] B. Park, K. Cho, B-M Moon, and S. Kim, Microelectronics Engineering 84 (2007) 1627.

Figure captions:

Fig. 1. Structure of sample with Al-rich Al₂O₃:

(a) cross section and (b) energy band diagram.

Fig. 2. C-V characteristics of Al-rich Al₂O₃ layer: (a) as-deposited and (b) annealed.

Fig. 3. Hysteresis voltage window vs. maximum applied gate voltage.

Fig. 4. Timewise change in capacitance for (a) as-deposited and (b) annealed samples.

Fig. 5. Change in flat-band voltage over time. The dashed line indicates ten years.

	[20]	[6]	[12]	This Work
Substrate type	p-Si	p-Si	n-Si	p-Si
$n_s (10^{13} \text{ cm}^{-2})$	1.29	0.65	0.64	2.14

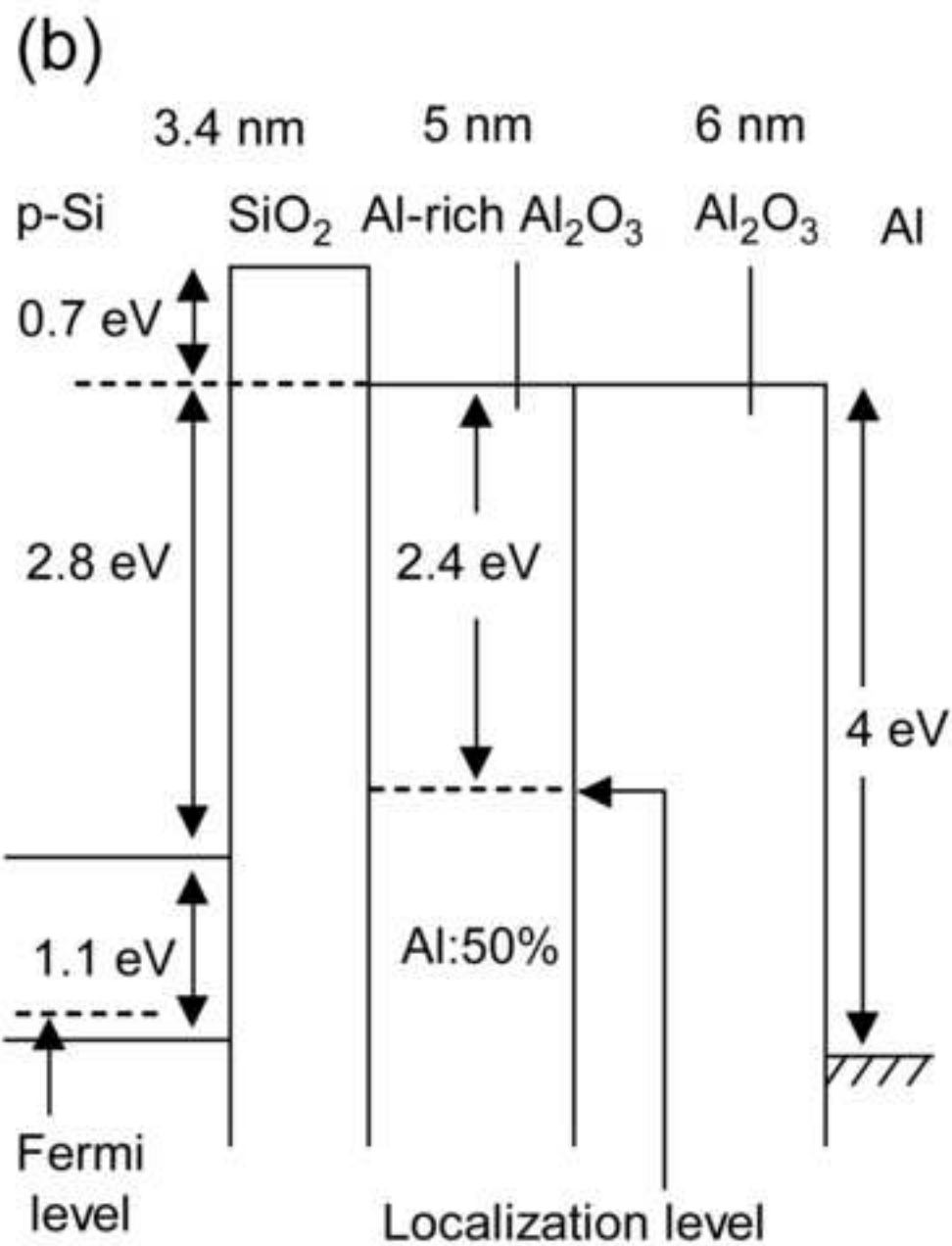
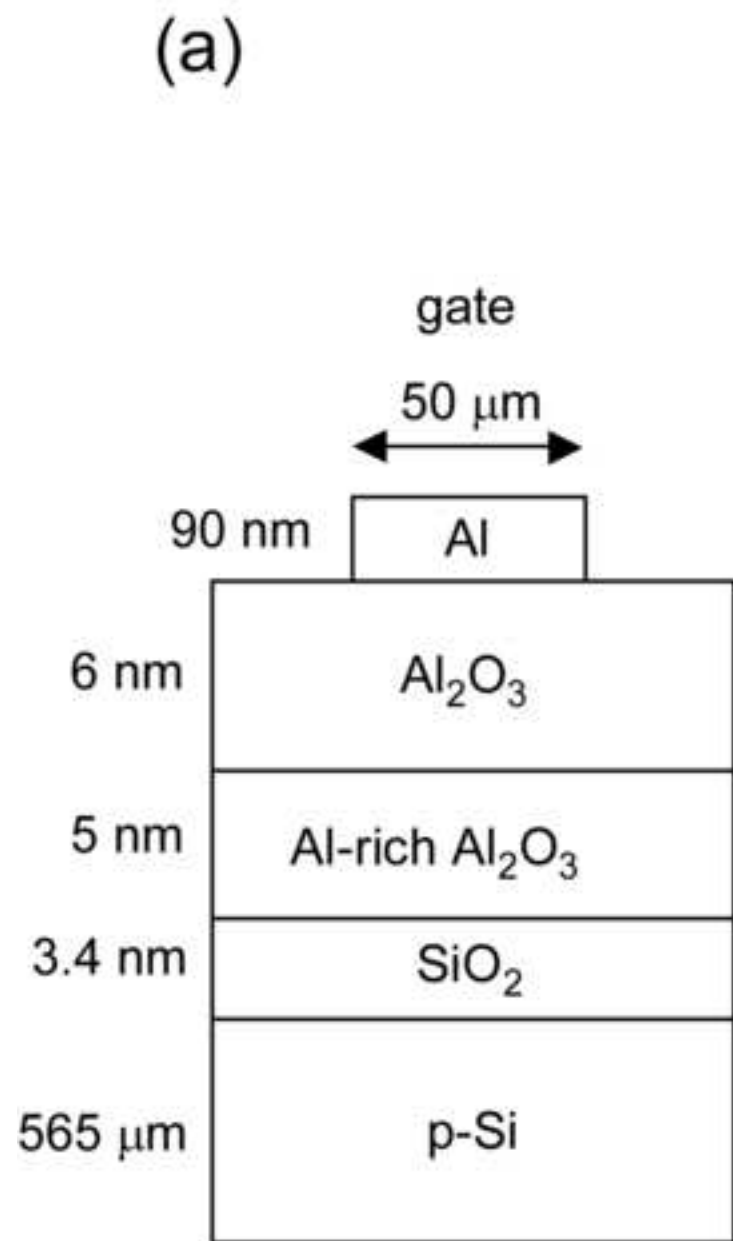


fig2
[Click here to download high resolution image](#)

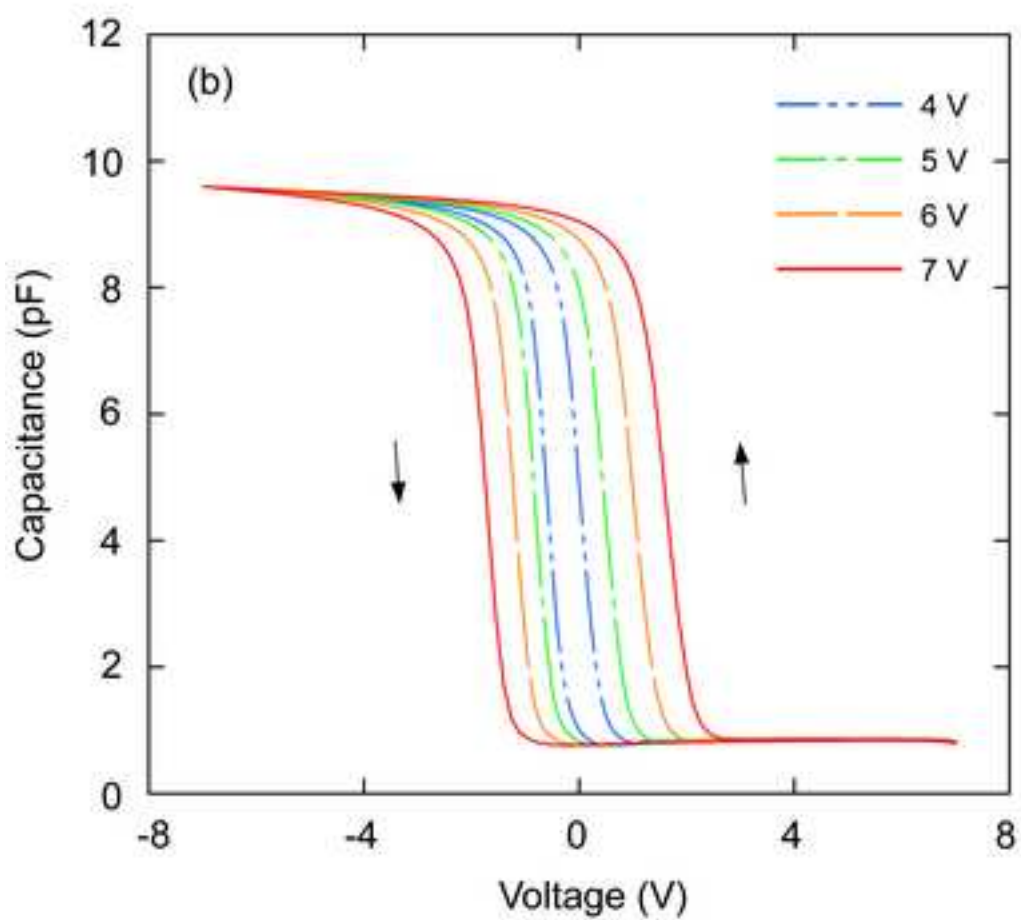
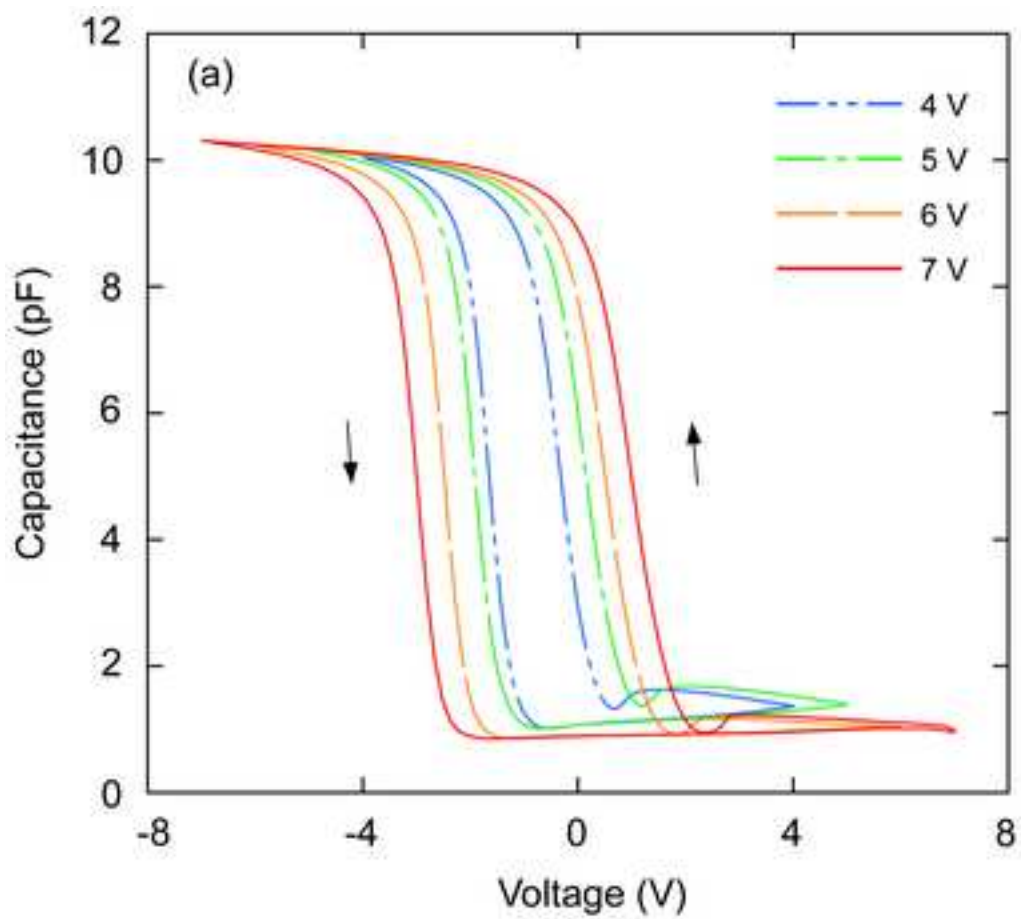


fig3
[Click here to download high resolution image](#)

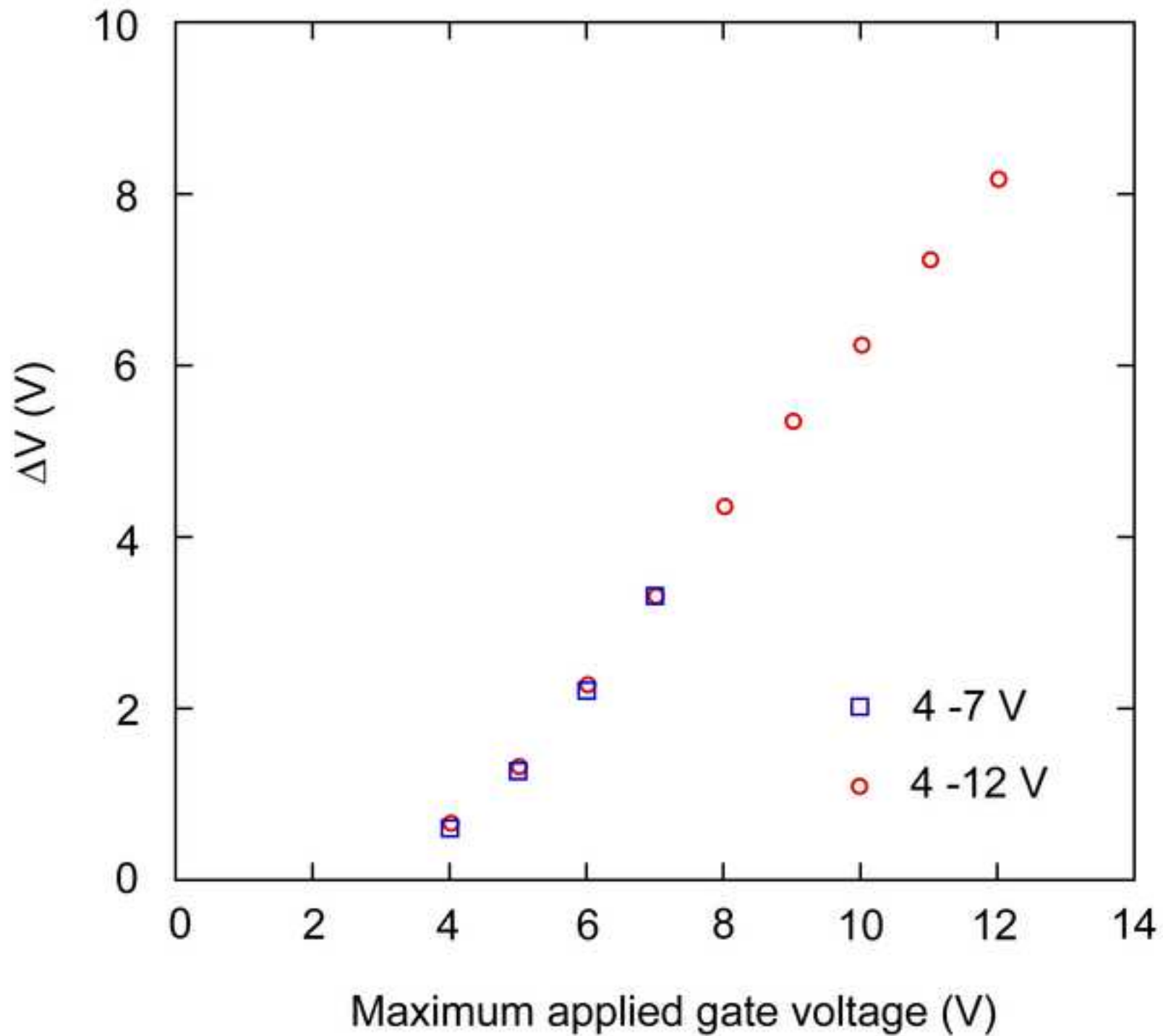


fig4
[Click here to download high resolution image](#)

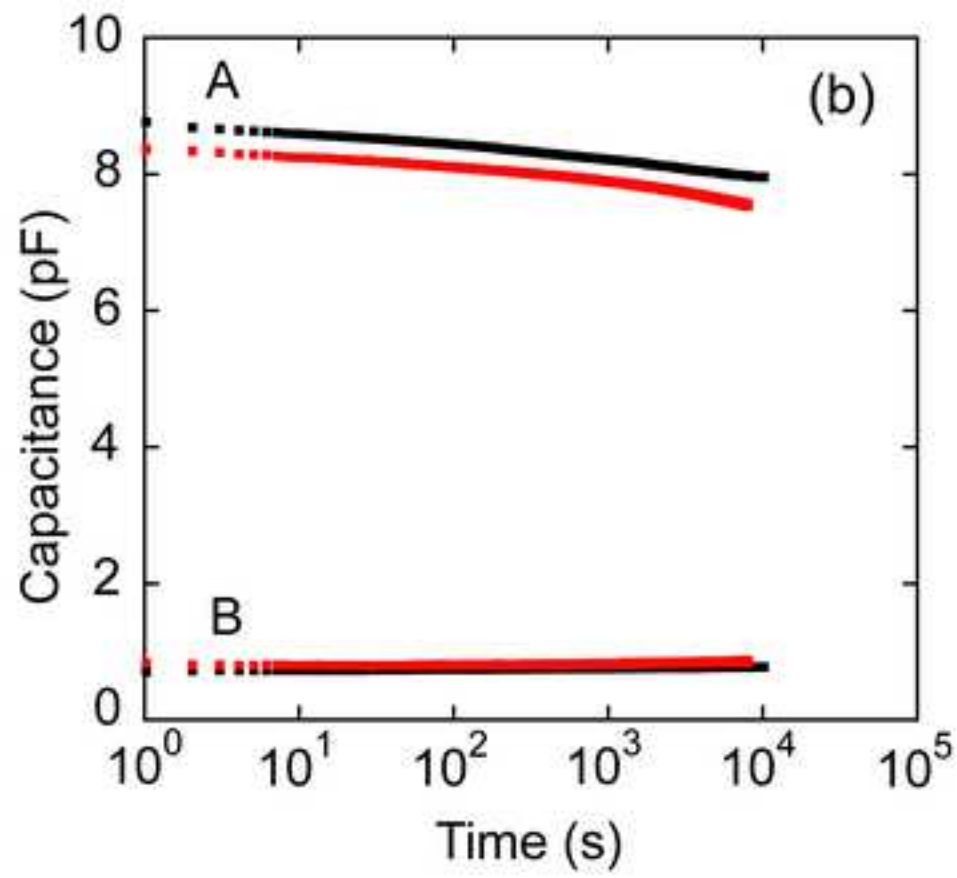
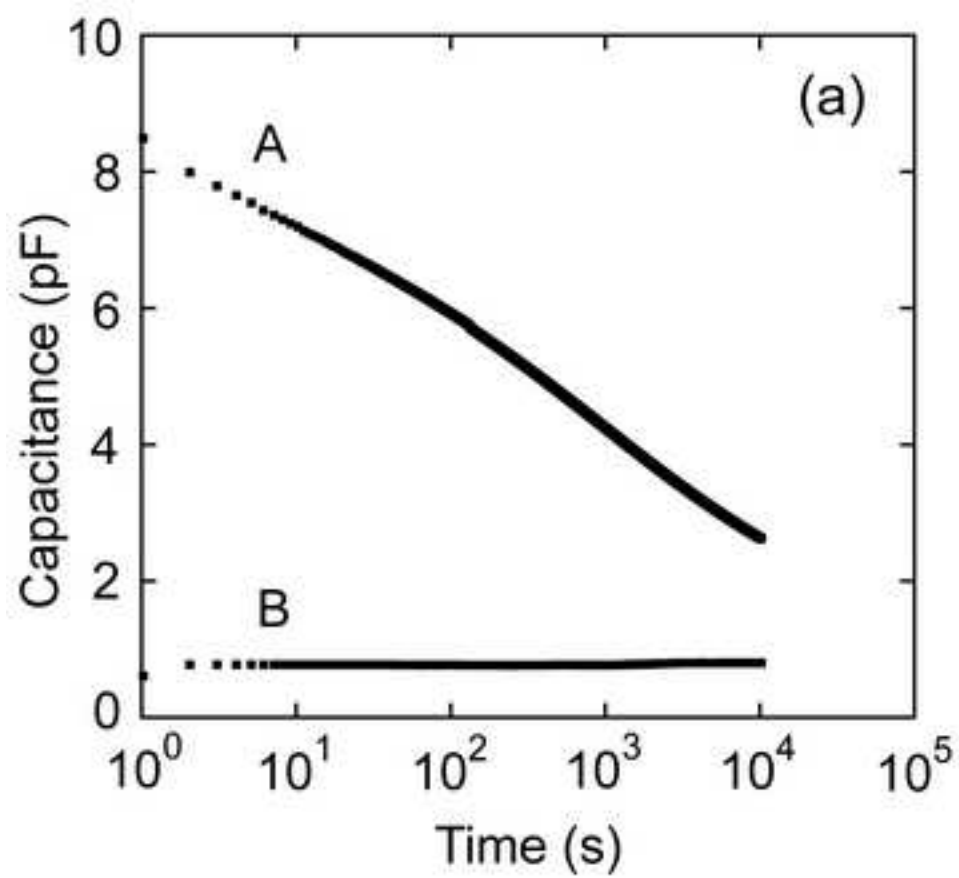


fig5

[Click here to download high resolution image](#)