Characterizing Silicon Avalanche Photodiode Fabricated by Standard 0.18□m CMOS Process for High-Speed Operation

PAPER

Characterizing Silicon Avalanche Photodiode Fabricated by Standard 0.18 μm CMOS Process for High-speed Operation

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SUMMARY nMOS-type and pMOS-type silicon avalanche photodiodes (APDs) were fabricated by standard 0.18 μm CMOS process, and the current-voltage characteristic and the frequency response of the APDs with and without guard ring structure were measured. The role of the guard ring is cancellation of photo-generated carriers in a deep layer and a substrate. The bandwidth of the APD is enhanced with the guard ring structure at a sacrifice of the responsivity. Based on comparison of nMOS-type and pMOS-type APDs, the nMOS-type APD is more suitable for high-speed operation. The bandwidth is enhanced with decreasing the spacing of interdigital electrodes due to decreased carrier transit time and with decreasing the detection area and the PAD size for RF probing due to decreased device capacitance. The maximum bandwidth was achieved with the avalanche gain of about 10. Finally, we fabricated a nMOS-type APD with the electrode spacing of 0.84 μm, the detection area of $10 \times 10\,\mu\text{m}^2$, the PAD size for RF probing of $30 \times 30\,\mu\text{m}^2$, and with the guard ring structure. The maximum bandwidth of 8.4 GHz was achieved along with the gain-bandwidth product of 280 GHz.

key words: *Photodiode, Avalanche photodiode, CMOS process, Silicon*

1. Introduction

Short-distance optical data transmission systems have been widely studied to realize board-to-board and chip-to-chip high-speed data transmission [1-3]. In these applications, short wavelength vertical-cavity surface-emitting lasers (VCSELs) and silicon (Si) photodiodes (PDs) are used for low-cost system configuration. Si PDs fabricated by CMOS process are promising optical devices for easy integration with electronic circuits without any process modification [4-6], and avalanche photodiodes fabricated by CMOS process (CMOS-APDs) have been developed for optical interconnection applications [7-10]. The bandwidth of the CMOS-APD, however, is limited by slow photo-generated carriers from the substrate because all the electrodes are arranged on the surface of the substrate. One solution is to add guard ring (GR) structure in the CMOS-APD [1,11]. We have studied CMOS-APDs with interdigital electrode structure for high-speed data transmission systems [12-13] and for Blu-ray optical disc system [14]. The CMOS-APDs with bandwidth over 1 GHz and the avalanche gain of more than 100 have been realized. We also reported 7 GHz-bandwidth CMOS-APD with the detection area of $20 \times 20\,\mu\text{m}^2$, the electrode spacing of 1 μm, and the PAD size for RF probing of $30 \times 30\,\mu\text{m}^2$ [15]. The dependence of the bandwidth on the detection area has been reported by Lee et al.[16] where enhancement of the bandwidth of the CMOS-APD up to 7.6 GHz was reported by reducing the device area to $10 \times 10\,\mu\text{m}^2$.

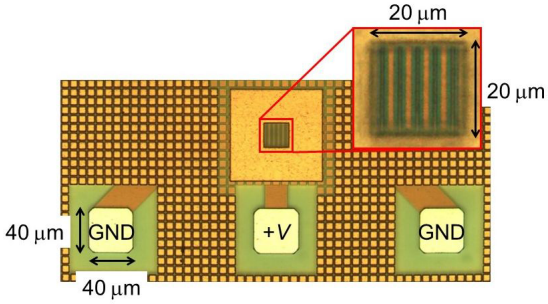

Fig. 1 Photograph of fabricate CMOS-APD.

In this paper, we will emphasize two main objectives; (1) investigation of the influence of the electrode spacing and the PAD size for RF probing as well as the detection area on the bandwidth of CMOS-APDs, and (2) discovering frequency response behavior of the CMOS-APDs at the low frequency region. By narrowing the electrode spacing to 0.84 μm, decreasing the detection area and the PAD size for RF probing to $10 \times 10\,\mu\text{m}^2$ and $30 \times 30\,\mu\text{m}^2$, respectively, the maximum bandwidth is enhanced to 8.4 GHz and the gain-bandwidth product of 280 GHz is achieved.

2. Structure

Figure 1 shows the photograph of the fabricated CMOS-APD. It has two parts that are the detection area and three PAD for RF probing and DC biasing. The detection area S_{DT} and the PAD size S_{PAD} are $S_{\text{DT}} = 20 \times 20\,\mu\text{m}^2$ and $S_{\text{PAD}} = 40 \times 40\,\mu\text{m}^2$, respectively.

Figure 2 shows the cross-sectional structure of (a) nMOS-type and (b) pMOS-type CMOS-APDs fabricated by standard 0.18 μm CMOS process without process modifications. The shallow trench isolation (STI) oxides are used as isolation regions between n^+-layer and p^+-layer. The n^+-layer and p^+-layer are arranged alternately and then the electrodes are interdigital structure with the electrode spacing, L_S. The light is illuminated from the top of the device.

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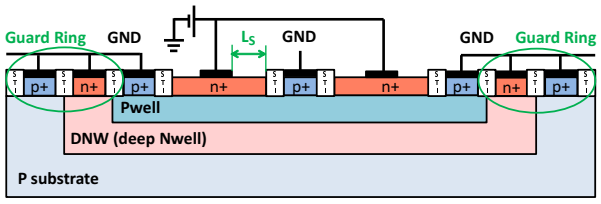
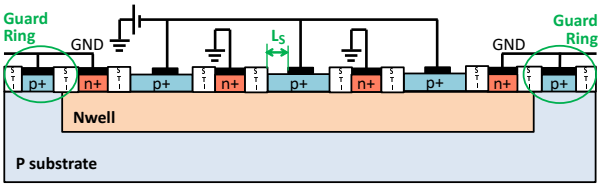


(a) nMOS-type CMOS-APD



(b) pMOS-type CMOS-APD

Fig. 2 Cross-sectional structure of fabricated CMOS-APDs.

From the figure, the difference between CMOS-APD with and without the GR structure is found to be the connection of electrodes of the P-substrate and the DNW to the ground in Fig. 2(a), and the connection of electrodes of the P-substrate to the ground in Fig. 2(b). If all electrodes are electrically shorted, it represents the existence of the GR. If not, the structure is without the GR structure, and the P-substrate and the DNW are open for the nMOS-type and the P-substrate is open for the pMOS-type.

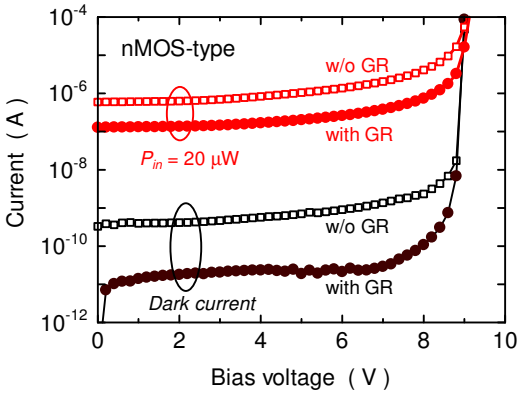
The structure of Fig. 2(a) is same with the nMOS structure in a P-substrate and then is referred to as the nMOS-type CMOS-APD. This structure was referred as the electron-injection-type CMOS-APD in our previous paper [13]. Due to the shorted GR, the photo-generated electrons in the P-substrate and DNW move toward n^+-layers on the DNW because of the built-in potential barrier between the Pwell and the DNW, while photo-generated holes in the P-substrate move toward the p^+-layers on the P-substrate because of the built-in potential barrier between the P-substrate and the DNW, and photo-generated holes in the DNW move toward the p^+-layer on the Pwell. They are recombined and do not contribute to the photocurrent. In the Pwell and the n^+-layer on the Pwell, the photo-generated electrons and holes are drifted towards the n^+-layers and the p^+-layers, respectively. Since the high electric field is applied between the n^+-layers and the Pwell, the photo-generated electrons in the Pwell and the photo-generated holes in the n^+-layer are multiplied due to avalanche mechanism while traveling toward the n^+-layer and the p^+-layer, respectively. As a result, the responsivity is enhanced. For the nMOS-type CMOS-APD without the GR, the potential barrier heights between the P-substrate and the DNW and between the DNW and the Pwell are undefined and may be low, and then the photo-generated electrons and holes in the P-substrate move toward the n^+-layers and the p^+-layers on the Pwell, respectively. Since the p^+-layers on the P-substrate and the n^+-layers on the DNW are not electrically connected, the photo-generated electrons and holes in the DNW and the P-substrate degrade high-speed operation because the carriers are slow diffusion carriers due to weak electric field.

The structure of Fig. 2(b) is same with the pMOS structure in a P-substrate and is referred to as the pMOS-type CMOS-APD. This structure was referred as the hole-injection-type CMOS-APD in our previous paper [13]. The photo-generated electrons in the P-substrate move to the n^+-layers on the Nwell, and the photo-generated holes move to the p^+-layers on the P-substrate due to the built-in potential barrier between the P-substrate and the Nwell, and they are recombined and do not contribute to the photocurrent. On the other hand, the photo-generated electrons in the Nwell and the p^+-layer on the Nwell drifted towards the n^+-layers, and the photo-generated holes in the Nwell drifted towards the p^+-layers on the Nwell, respectively. In this region, a high electric field is applied between p^+-layers and Nwell, and therefore, the photo-generated electrons in the p^+-layer and the photo-generated holes in the Nwell are multiplied due to avalanche mechanism while traveling toward the n^+-layer and the p^+-layer, respectively. As a result, the responsivity is enhanced. For the pMOS-type CMOS-APD without the GR, the potential barrier height between the P-substrate and the Nwell are undefined and may be low, and then the photo-generated electrons and holes in the P-substrate move toward the n^+-layers and the p^+-layers on the Nwell, respectively. Since the p^+-layers on the P-substrate are not electrically connected together with the n^+-layers on the Nwell to the ground, the photo-generated electrons and holes in the P-substrate degrade high-speed operation because the carriers are slow diffusion carriers due to weak electric field.

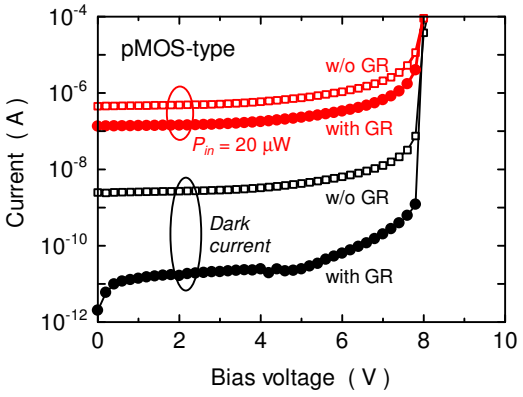
3. *I–V* Characteristics and Responsivity

In the measurement, a laser light from a 10 Gbps vertical cavity surface emitting laser (VCSEL) at 850 nm wavelength was intensity modulated and was illuminated from the top of the device. The electrode spacing L_S, the detection area S_{DT} and the PAD size S_{PAD} are 1.0 μm, 20×20 μm^2 and $40 \times 40\,\mu m^2$, respectively.

Figure 3 shows the measured *I–V* characteristics for (a) nMOS-type and (b) pMOS-type CMOS-APDs with and without the GR. The dark current at a low bias is about 10 pA with the GR structure, and the dark current without the GR structure is higher than that with the GR structure. It is because the carriers in the deep layer and the substrate are canceled due to the GR structure and are not canceled in the CMOS-APD without the GR structure. The breakdown voltage measured when the dark current exceeds 1 μA is about 9.05 V and 8 V for the nMOS-type and the pMOS-type, respectively. The breakdown voltage difference for those types may be caused by different doping concentration in the Pwell and the Nwell, which are not disclosed from the manufacturer. Under light illumination at 20 μW, the photocurrent is almost constant for low bias voltage for both types, and it is gradually increased and finally is significantly increased before breakdown voltage due to avalanche



(a) nMOS-type CMOS-APD.



(b) pMOS-type CMOS-APD.

Fig. 3 *I–V* characteristics of CMOS-APDs with and without GR. The electrode spacing $L_S = 1.0\,\mu$m and the detection area $S_{\mathrm{DT}} = 20 \times 20\,\mu\mathrm{m}^2$.

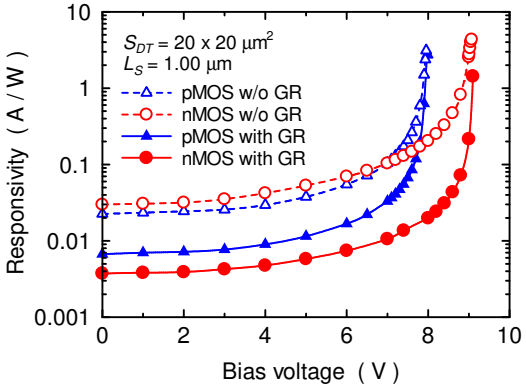


Fig. 4 Responsivity against bias voltage of CMOS-APDs.

amplification.

Figure 4 shows the responsivity of the nMOS-type and the pMOS-type CMOS-APDs with and without the GR as a function of the bias voltage. The responsivity rises initially with the bias voltage because of the increase of the depletion width. It is then dramatically increased at a certain voltage due to avalanche amplification, and the responsivity more than 1 A/W is achieved near the breakdown voltage for all the devices. The responsivity of the CMOS-APDs with the GR is lower than that of without the GR because the quantum efficiency is decreased due to cancellation of photo-generated carries in the deep layer and the P-substrate.

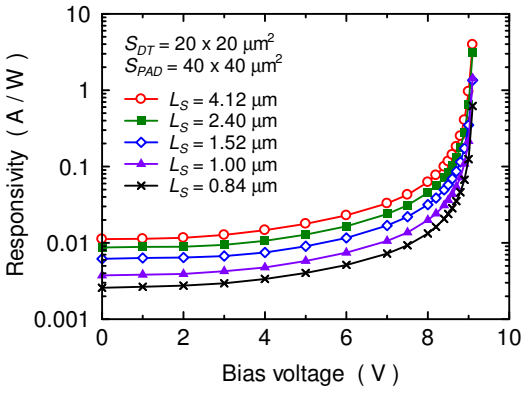


Fig. 5 Responsivity of nMOS-type CMOS-APDs with the GR for different electrode spacing L_S.

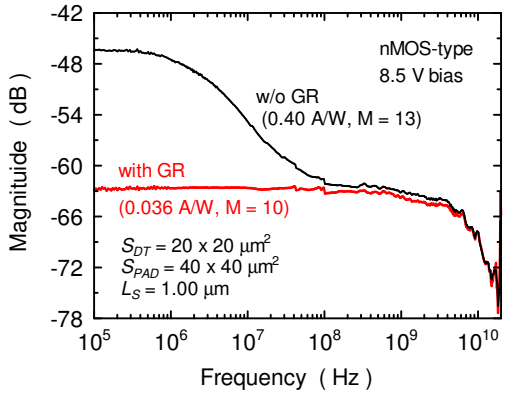
Figure 5 shows the responsivity of the nMOS-type CMOS-APDs with the GR for different electrode spacing L_S. The detection are S_{DT} and the PAD size S_{PAD} are $20 \times 20\,\mu\mathrm{m}^2$ and $40 \times 40\,\mu\mathrm{m}^2$, respectively, for all the device. The responsivity is increased with increasing the electrode spacing because the number of electrode is decreased with increasing the electrode spacing and then the effective illuminating area is increased.

4. Frequency Response

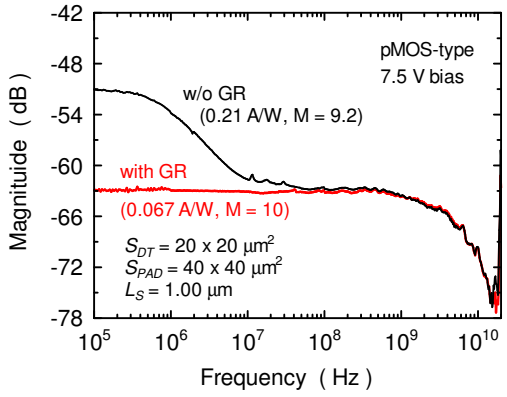
The frequency response was measured by using two types of network analyzers; Hewlett Packard 4396A for low frequency range of 100 kHz to 1 GHz, and Agilent Technology E8363B for a high frequency range of 10 MHz to 40 GHz. The frequency responses of the VCSEL and RF cables are compensated by using a commercial GaAs PIN photodiode with the nominal bandwidth of 30 GHz (Albis Optoelectronics AG, PQW30A-S).

Figure 6 shows the frequency response for (a) nMOS-type and (b) pMOS-type CMOS-APD for 8.5 V and 7.5 V bias voltage, respectively, at 850 nm wavelength. The frequency response for the CMOS-APD with the GR is flat until several GHz. On the other hand, the frequency response of the CMOS-APD without the GR shows high signal magnitude for low frequency region and then dropped to the same signal magnitude with the GR structure around 100 MHz. The large signal magnitude of about 15 dB as compared to the CMOS-APD with the GR at low frequency is due to slow diffusion carriers from the deep layer and the P-substrate. The bandwidth of the CMOS-APD with the GR is three orders of magnitude wider as compared to the CMOS-APD without the GR due to cancellation of photo-generated carriers in the deep layer and the P-substrate which are slow diffusion carriers.

The comparison of the frequency response between nMOS-type and pMOS-type CMOS-APDs with the GR is



(a) nMOS-type CMOS-APD.



(b) pMOS-type CMOS-APD.

Fig. 6 Frequency response of CMOS-APDs with and without GR.

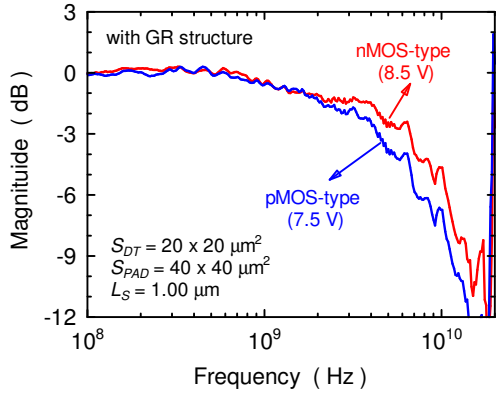
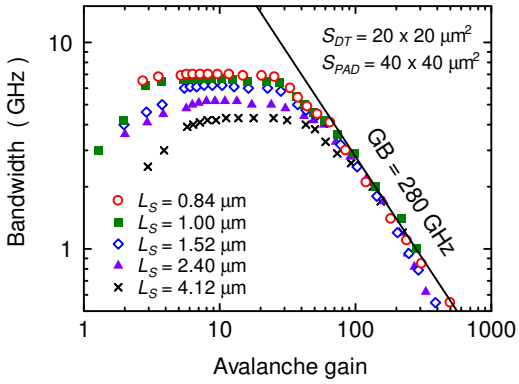


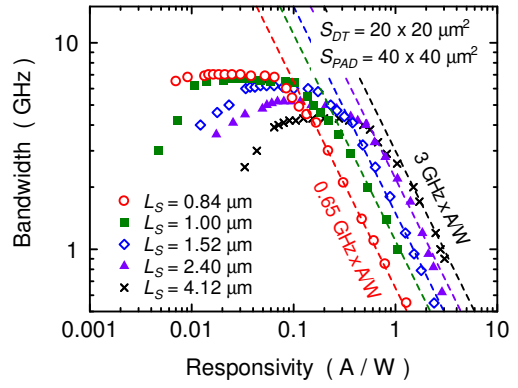
Fig. 7 Comparison of frequency response of nMOS-type and pMOS-type CMOS-APD with GR.

shown in Fig. 7. From the normalized frequency response, the maximum bandwidth for nMOS-type CMOS-APD is 6.77 GHz and is higher than the pMOS-type CMOS-APD of 4.29 GHz. It is due to the quicker avalanche buildup time of electrons compared to the holes, or in other words, the electrons move faster in Pwell rather than holes in Nwell. Therefore we conclude that the nMOS-type CMOS-APD with the GR is suitable for high-speed application.

Then we discuss detailed experimental results on the



(a) Relation between avalanche gain and bandwidth.



(b) Relation between responsivity and bandwidth.

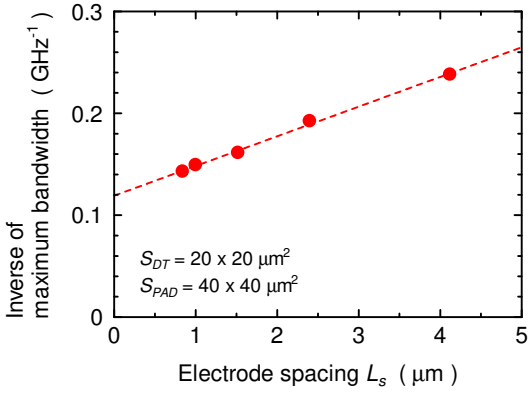
Fig. 8 Relation between avalanche gain and bandwidth and relation between responsivity and bandwidth of the nMOS-type CMOS-APDs with GR for different electrode spacing L_S.

bandwidth of nMOS-type CMOS-APDs with the GR for various electrode spacing L_S, the detection area S_{DT}, and the PAD size S_{PAD}. The idea is that the bandwidth can be improved by reducing the carrier transit time due to decreasing the electrode spacing L_S. Bandwidth enhancement can be also achieved by shrinking the detection area and the PAD size for RF probing due to decreased depletion capacitance and the PAD capacitance, respectively.

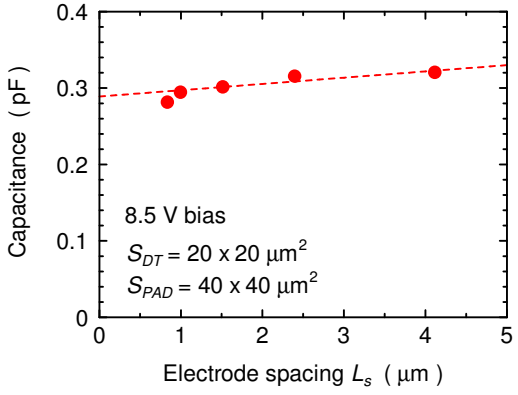
Figure 8(a) shows the relation between the avalanche gain and the bandwidth of the CMOS-APDs for different electrode spacing L_S. The detection area S_{DT} and the PAD size S_{PAD} are $S_{\mathrm{DT}} = 20 \times 20\,\mu\mathrm{m}^2$ and $S_{\mathrm{PAD}} = 40 \times 40\,\mu\mathrm{m}^2$, respectively. The bandwidth is enhanced with decreasing the electrode spacing and is maximized when the avalanche gain is about 10 irrespective of the electrode spacing L_S. The maximum bandwidth of 7 GHz is obtained when the avalanche gain is about 10 for the electrode spacing $L_S = 0.84\,\mu$m. The gain-bandwidth product is the same irrespective of the electrode spacing L_S and is 280 GHz. Figure 8(b) shows the relation between the responsivity and the bandwidth of the CMOS-APDs for different electrode spacing L_S. Since the responsivity depends on the electrode spacing L_S as shown in Fig. 5, the responsivity-bandwidth product also depends on the electrode spacing L_S, and the value is tabulated in Table 1. Commercial fast Si PIN-PD typically

Table 1 Gain-bandwidth product and responsivity-bandwidth product of nMOS-type CMOS-APDs with the GR.

Electrode spacing L_S (μm)	Gain-bandwidth product (GHz)	Responsivity-bandwidth product (GHz × A/W)
0.84	280	0.65
1.00	280	1.1
1.52	280	1.5
2.40	280	2.2
4.12	280	3.0



(a) Relation between electrode spacing and maximum bandwidth.



(b) Relation between electrode spacing and capacitance.

Fig. 9 Electrode spacing dependence of maximum bandwidth and device capacitance of the CMOS-APD.

has the responsivity of 0.4 ~ 0.5 A/W and the bandwidth of 1 ~ 2 GHz, and the CMOS-APD has wider bandwidth and higher responsivity as compared to commercial Si PIN-PDs at a same bias voltage (below 10 V).

Figure 9(a) shows the relation between the inverse of the maximum bandwidth and the electrode spacing obtained from Fig. 8(a). The inverse of the maximum bandwidth is proportional to the electrode spacing L_S, and the maximum bandwidth is estimated to be about 8.4 GHz, which is derived from the electrode spacing $L_S = 0\,\mu$m. Figure 9(b) shows the device capacitance of the CMOS-APDs at 8.5 V bias voltage against the electrode spacing L_S measured by a LCR meter (Agilent 4284A Precision LCR meter) at 1 MHz. The device capacitance includes depletion capacitance of p-n junctions and the PAD capacitance, and is about 300 fF.

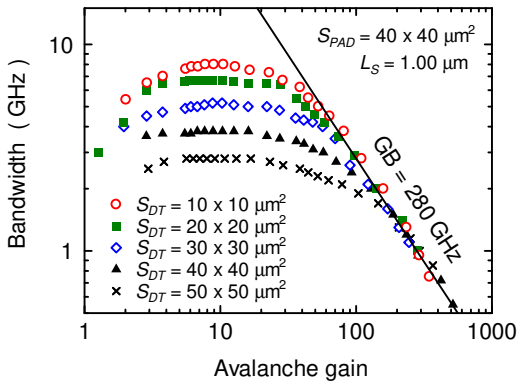


Fig. 10 Relation between avalanche gain and bandwidth of the CMOS-APDs for different detection area S_{DT}.

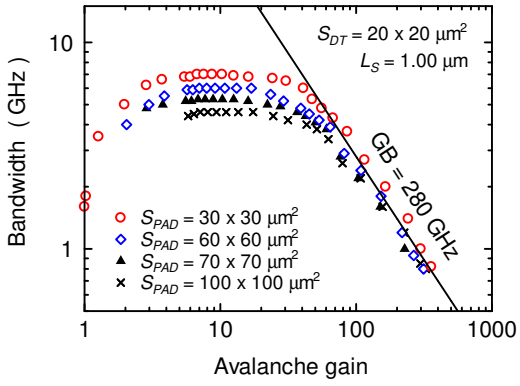
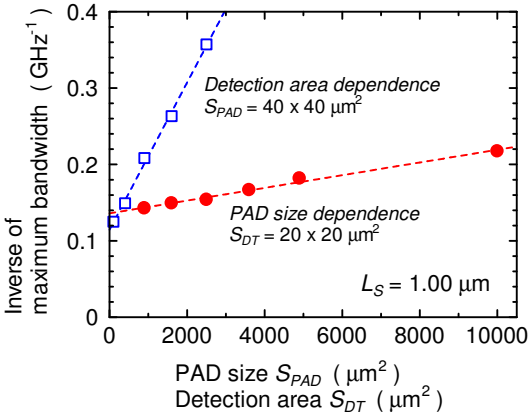


Fig. 11 Relation between avalanche gain and bandwidth of the CMOS-APDs for different PAD size S_{PAD}.

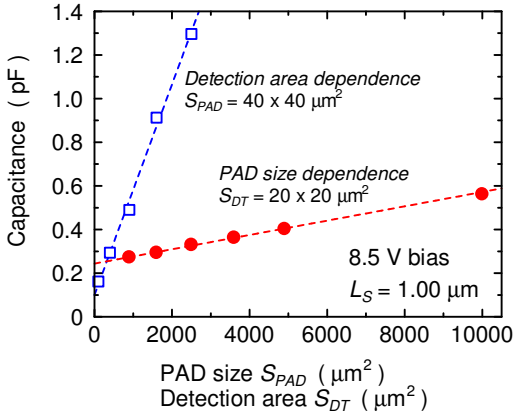
The device capacitance is slightly decreased with decreasing the electrode spacing L_S. This is due to decreased total area of the p-n junction between n^+- and Pwell layers because the number of electrodes is increased due to decreased electrode spacing with constant detection area S_{DT}. However the dependence of the device capacitance on the electrode spacing is very weak, and then the bandwidth enhancement with decreasing the electrode spacing shown in Fig. 9(a) is due to decreased carrier transit time owing to electrode spacing narrowing.

Figure 10 shows the relation between the avalanche gain and the bandwidth for different detection area S_{DT}. The electrode spacing L_S and the PAD size S_{PAD} are $L_S = 1.00\,\mu$m and $S_{\mathrm{PAD}} = 40 \times 40\,\mu\mathrm{m}^2$, respectively. The detection area of $10 \times 10\,\mu\mathrm{m}^2$ shows the largest bandwidth of about 8.0 GHz compared to other sizes. It means that, the smaller detection area enhances the bandwidth, however, too-small detection area causes difficulty of light illumination from top of the CMOS-APD. Figure 11 shows the relation between the avalanche gain and the bandwidth for different PAD size S_{PAD}. The electrode spacing L_S and the detection area S_{DT} are $L_S = 1.00\,\mu$m and $S_{\mathrm{DT}} = 20 \times 20\,\mu\mathrm{m}^2$, respectively. The bandwidth is increased with decreasing the PAD size.

From Figs. 8(a), 10, and 11, the bandwidth is found to



(a) Maximum bandwidth



(b) Device capacitance

Fig. 12 Dependence of maximum bandwidth and device capacitance on detection area and PAD size.

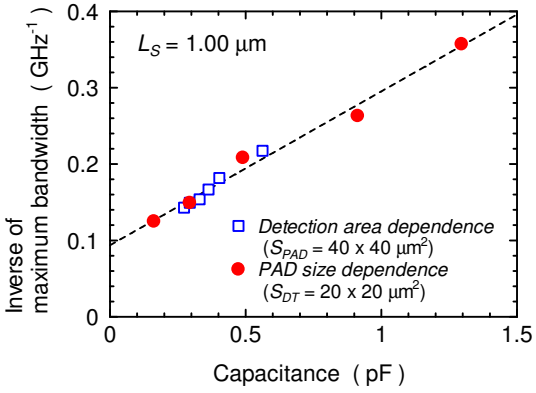


Fig. 13 Relation between the device capacitance and the inverse of the maximum bandwidth of the CMOS-APDs.

be inversely proportional to the avalanche gain larger than 100, and the gain-bandwidth (GB) product is 280 GHz irrespective of the electrode spacing, the detection area, and the PAD size.

Figure 12(a) shows the relation between the inverse of the maximum bandwidth and the detection area S_{DT} and the PAD size S_{PAD} obtained from Figs. 10 and 11. The open squares are the inverse of the maximum bandwidth against the detection area S_{DT} with the PAD size $S_{\mathrm{PAD}} = 40 \times 40\,\mu\mathrm{m}^2$, and the closed circles are the inverse of the maximum bandwidth against the PAD size S_{PAD} with the detection area $S_{\mathrm{DT}} = 20 \times 20\,\mu\mathrm{m}^2$. The inverse of the maximum bandwidth is proportional to both the detection area and the PAD size. Figure 12(b) shows the device capacitance of the CMOS-APDs at 8.5 V bias voltage against the detection area S_{DT} and the PAD size S_{PAD} measured by a LCR meter (Agilent 4284A Precision LCR meter) at 1 MHz. The device capacitance is linearly decreased with decreasing the detection area S_{DT} and the PAD size S_{PAD}. The PAD capacitance for $S_{\mathrm{PAD}} = 40 \times 40\,\mu\mathrm{m}^2$ is estimated to be 100 fF from $S_{\mathrm{DT}} = 0\,\mu\mathrm{m}^2$, and the depletion capacitance of the detection area of $20 \times 20\,\mu\mathrm{m}^2$ is estimated to be 244 fF from $S_{\mathrm{PAD}} = 0\,\mu\mathrm{m}^2$. The dependence of the device capacitance on the detection area S_{DT} and the PAD size S_{PAD} is almost the same with Fig. 12(a). As a result, the bandwidth enhancement with decreasing the detection area and the PAD size shown in Fig. 12(a) is due to decreased device capacitance owing to decreased detection area S_{DT} and the PAD size S_{PAD}.

Figure 13 shows the relation between the device capacitance and the inverse of the maximum bandwidth derived from Figs. 12(a) and (b). The open squares are the inverse of the maximum bandwidth for different detection area S_{DT} with the PAD size $S_{\mathrm{PAD}} = 40 \times 40\,\mu\mathrm{m}^2$, and the closed circles are the inverse of the maximum bandwidth for different PAD size S_{PAD} with the detection area $S_{\mathrm{DT}} = 20 \times 20\,\mu\mathrm{m}^2$. The inverse of the maximum bandwidth is linearly changed with the device capacitance, and then the bandwidth enhancement with decreasing the detection area and the PAD size is due to the decrease of the device capacitance. It is also found that the ultimate bandwidth is estimated to be about 10.7 GHz from the y-intercept. This bandwidth is determined by carrier transit time, and then the bandwidth can be enhanced to decrease the electrode spacing at the sacrifice of the responsivity because decreased electrode spacing increases the number of electrode and then the effective illuminating area is decreased.

Finally, we fabricated a nMOS-type CMOS-APD with the electrode spacing of 0.84 μm, the detection area of $10 \times 10\,\mu\mathrm{m}^2$ and the PAD size for RF probing of $30 \times 30\,\mu\mathrm{m}^2$ along with the guard ring structure for the purpose of high-speed operation. The detection area is determined to effectively illuminate a laser light guided by using a SI-9 optical fiber, and the PAD size is determined to match the tip size of the RF probe. The relation between the avalanche gain and the bandwidth is shown in Fig. 14. The maximum bandwidth of 8.4 GHz, the gain-bandwidth product of 280 GHz, and the responsivity-bandwidth product of 0.7 GHz $\times$ A/W are achieved. The maximum bandwidth is achieved at the avalanche gain of about 10 and the responsivity of about 0.02 A/W.

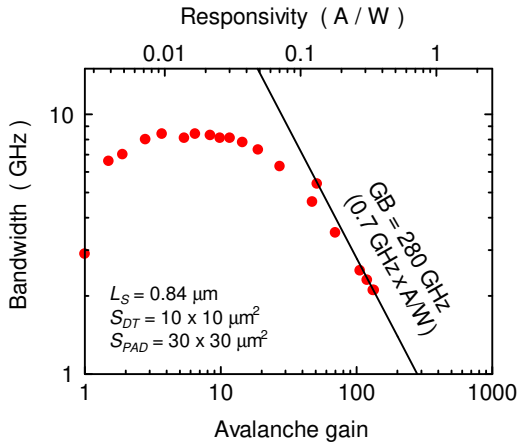


Fig. 14 Relation between avalanche gain and the bandwidth of the CMOS-APDs.

5. Conclusions

nMOS-type and pMOS-type CMOS-APDs with and without guard ring (GR) are fabricated by standard 0.18 μm CMOS process without process modification. The responsivity of the CMOS-APD with the GR is lower than the CMOS-APD without the GR because the quantum efficiency is decreased due to cancellation of carriers photo-generated in the deep layer and the P-substrate. However, the maximum bandwidth for the CMOS-APD with the GR is wider as compared to the CMOS-APD without the GR due to cancellation of photo-generated carriers in the deep layer and the substrate because the carriers are slow diffusion carriers. The nMOS-type CMOS-APD is faster than the pMOS-type CMOS-APD and is suitable for high-speed application. By optimizing the electrode spacing to 0.84 μm, decreasing the detection area and the PAD size for RF probing to $10 \times 10\,\mu\text{m}^2$ and $30 \times 30\,\mu\text{m}^2$, respectively, the maximum bandwidth of a CMOS-APD is enhanced to 8.4 GHz with the gain-bandwidth product of 280 GHz and the responsivity-bandwidth product of 0.7 GHz $\times$ A/W.

Acknowledgments

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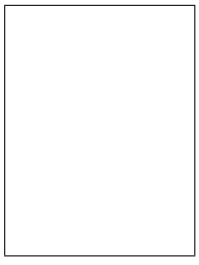

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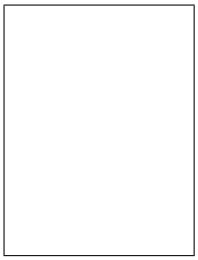

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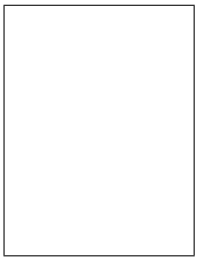

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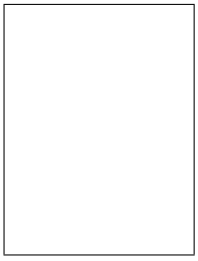

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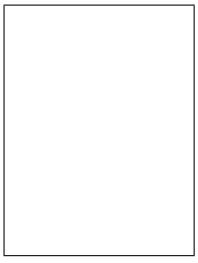

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