

Column-Parallel Architecture for Line-of-Sight Detection Image Sensor Based on Centroid Calculation

Hayato Kawakami[†], Satoru Igarashi[†], Yuta Sasada[†], Junichi Akita[†] (member)

Abstract Line-of-sight (LoS) detection is used for various user-interfaces, and a rapid eye movement, which is called saccade, is expected to be applied to new user-interfaces. The authors propose the column-parallel architecture for LoS detection image sensor to realize the high frame rate of 1,000[fps] and 640 x 480[pixels] resolution. An emulation system using a high speed camera and FPGA was developed for algorithm evaluation, operating at 1,000[fps] and succeeded to track saccade movement. In addition, the preliminary integrated image sensor with 16 x 16[pixels] has been designed.

Keywords: Line-of-sight, Saccade, Pupil, Column-parallel architecture, Centroid calculation, Integrated image sensor

1. Introduction

Line-of-sight (LoS) detection, or detecting where the user is looking at, is expected as a new type of user interfaces¹⁾. The eyeball often moves very rapidly, which is called as saccade, and it is also expected to be applied for another type of user-interfaces²⁾. However, real-time tracking of saccade is difficult with the conventional image processing systems for their long processing time and latency against the speed of saccade, whose speed reaches up to 700[deg/sec], which required frame rate of over 200[fps] to capture³⁾. There are several LoS detection systems with the high frame rate to capture the saccade, however, their output latency, or the processing time to obtain the result, is several frames⁴⁾, and they can not track the saccade in real time.

In this paper, we propose the column-parallel LoS detection architecture for the integrated image sensor, which has a capability to track the saccade, as well as its implementation on the emulation system using a high speed camera and FPGA. The column-parallel architecture is employed to achieve both high resolution and high frame rate, both of them are enough for the practical LoS detection applications. The pixel parallel architecture, where the processing is performed in each pixel, requires the large circuit area in each pixel, which results in low resolution, while it achieves the high

processing speed. We also describe the preliminary design of the integrated image sensor using the proposed architecture.

2. LoS Calculation

The LoS can be calculated from the position of the pupil in the infrared image of the user's eye, which is observed as a black area⁵⁾, as shown in **Fig. 1**. The position of the pupil, whose shape is a circle, can be defined as a centroid of the pupil (digitized black) area with the sub-pixel accuracy.

The centroid of the area, (\bar{x}, \bar{y}) with the binary flag of p_{xy} for the pixel composing the pupil area, can be calculated as follows.

$$\left(\bar{x} = \frac{\sum_x \sum_y x p_{xy}}{\sum_x \sum_y p_{xy}}, \bar{y} = \frac{\sum_x \sum_y y p_{xy}}{\sum_x \sum_y p_{xy}} \right) \quad (1)$$

As shown in eq. (1), the values of $\sum_x \sum_y p_{xy}$, $\sum_x \sum_y x p_{xy}$, and $\sum_x \sum_y y p_{xy}$ are required in calculation of the centroid.

Note that the pupil may be occluded by an eyelid if the user sees the upper or the lower area. This phenomenon results in the error of the calculated pupil's centroid against the actual pupil position calculation, however, it

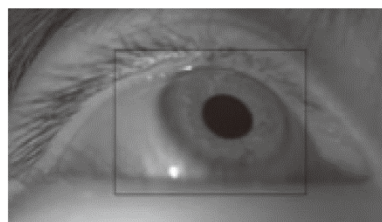


Fig.1 Example of an infrared image of eye.

Received August 31, 2013; Revised November 28, 2013; Accepted December 26, 2013

[†] Kanazawa University
(Ishikawa, Japan)

can be compensated with the calibration operation in advance to the usage.

3. Column-Parallel Architecture for Centroid Calculation

3.1 Outline of the architecture

Fig. 2 and **Fig.3** show the designed the column-parallel architecture for the centroid calculation, to realize both the high resolution, such as VGA (640 x 480[pixels]) or above, and the high frame rate, such as 500[fps] or above⁶⁾. Fig.2 shows the whole architecture of an integrated image sensor, where the array of pixel circuit APS (Active Pixel Sensor) forms the pixel plain, and Fig. 3 shows a processing element (PE) for one column. The S, SX, and SY are the circuits for calculating $\sum_y p_{xy}$, $\sum_y xp_{xy}$, and $\sum_y yp_{xy}$, respectively, and they are composed of one bit element circuits, Su, SXu, and SYu, respectively. The subscripts of the variables of S, SX, and SY in Fig. 3 indicate the number of bit order. For example, the combination of $\{S_{n-1}, \dots, S_1, S_0\}$ represents the n-bit binary expression of the output of circuit S, or the calculated area. The combinations of $\{X_{n-1}, \dots, X_1, X_0\}$ and $\{Y_{n-1}, \dots, Y_1, Y_0\}$ represent the binary expressions of the input of X- and Y-coordinates, respectively. The C_i and C_o are carry-in and carry-out of one bit full-adder placed in Su, SXu, and SYu.

Fig. 4 shows the pixel circuit. The photo diode in each pixel is first reset in each frame, and then the photo current is integrated during the defined exposure time, which generates the voltage decrease according to the photo intensity. The flag to indicate the pixel contained in the pupil area, p_{xy} , is generated by a voltage comparator with adequate threshold in each column at the certain timing for each sequential readout step in entire row from pixel circuits.

The calculation of $\sum_x \sum_y p_{xy}$, $\sum_x \sum_y xp_{xy}$, and $\sum_x \sum_y yp_{xy}$ are performed in parallel at each column.

The sum of the horizontal (X-) and the vertical (Y-) directions, $\sum_x \sum_y$ can be separated into Y-direction (\sum_y) and X-direction (\sum_x), and Y-direction sum, \sum_y , can be calculated at the sequential readout step for entire rows independently in each column.

After finishing readout step for Y-direction in each column, the calculation of \sum_x is performed with reading out the Y-direction accumulation result in each column in order, and accumulating them for all the columns, which are performed by the accumulator circuit located outside the column array as shown in Fig. 2. **Fig. 5** shows the operation timing of image transfer and

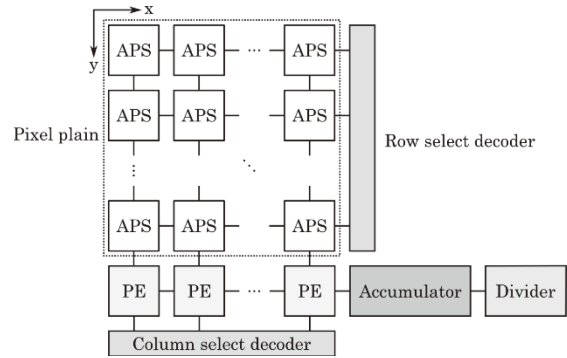


Fig.2 Column-parallel architecture of centroid calculation for integrated image sensor.

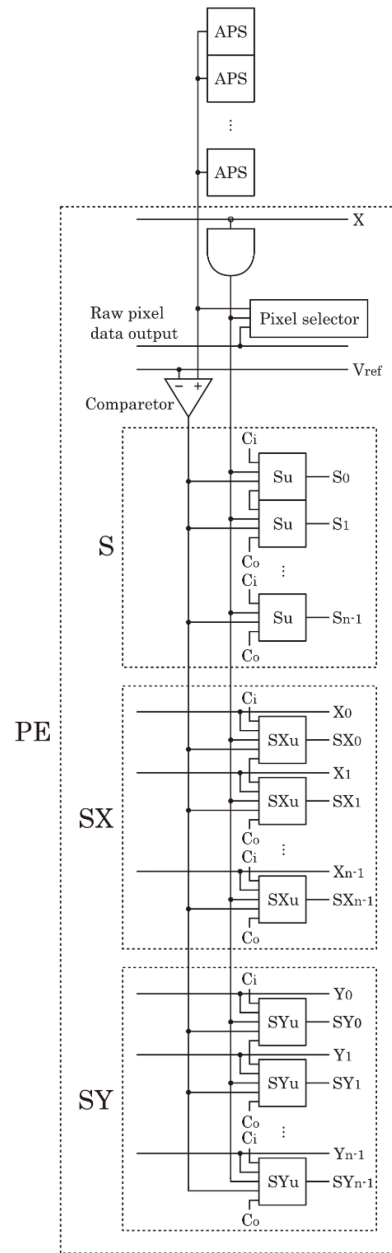


Fig.3 The circuit of column-parallel architecture for centroid calculation (for one column).

centroid calculation of this architecture. Since the centroid calculation is performed in parallel at each column, and the following step over all the columns, the

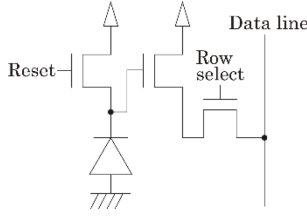


Fig.4 The circuit of CMOS active pixel image sensor.

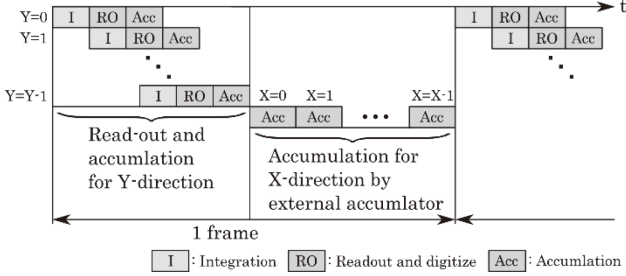


Fig.5 The operation timing of image transfer and calculation.

total number of operation steps, $(N_Y + N_X)$, where N_X and N_Y are the horizontal and vertical number of pixels, respectively. The required operation frequency of the calculation circuit, f , is expressed as follows.

$$f = F \cdot (N_Y + N_X) \quad (2)$$

Here, F is the frame rate. From eq. (2), the frame rate of 500[fps] and VGA resolution (640 x 480[pixels]) give f of 560[kHz], which can be easily achieved by the recent CMOS technologies.

The expected maximum number of the values of $\sum_x \sum_y p_{xy}$, $\sum_x \sum_y x p_{xy}$, and $\sum_x \sum_y y p_{xy}$ in each column are N_Y , $(N_X - 1)N_Y$, and $N_Y(N_X - 1)/2$, respectively for the case of all the p_{xy} is equal to '1', and they define the maximum number of bits of circuits S, SX, and SY, respectively. The circuit area of one column processing element is expressed as follows.

$$A_S \cdot [\log_2 N_Y] + A_{SX} \cdot [\log_2 (N_X - 1)N_Y] + A_{SY} \cdot \left[\log_2 \frac{N_Y(N_Y - 1)}{2} \right] \quad (3)$$

Here, A_S , A_{SX} , and A_{SY} are the area of one bit circuits of Su, SXu, and SYu, respectively, and it is proportional to $O(\log_2 N)$, where N is the number of pixels in one edge, which occupies relatively small area compared to the pixel plain with increased number of pixels.

3.2 Calculation of $\sum_x \sum_y p_{xy}$

The circuit of calculating $\sum_y p_{xy}$ at each column, which is indicated as "S" in Fig. 3, is composed of the pairs of one bit element circuit, Su. One Su is composed of one bit full-adder (FA), register (REG), and tri-state buffer (BUF), as shown in Fig. 6. The serial connection of Su forms a ripple-carry adder and the accumulation register for the required number of bits in calculations, as shown

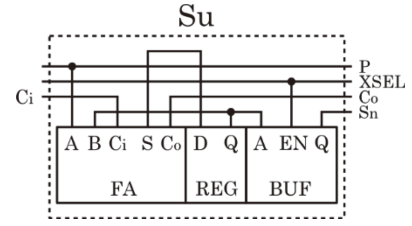


Fig.6 The 1-bit circuit of $\sum_y p_{xy}$ calculation, Su.

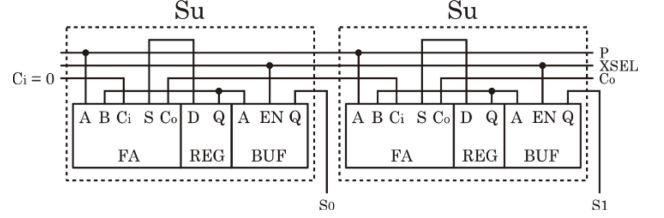


Fig.7 Example of 2-bit S circuit.

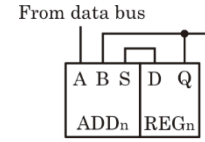


Fig.8 The circuit of column-direction accumulation.

in Fig. 7.

The binary flag to indicate the pupil area pixel from the voltage comparator, P , gives the value of P , and is accumulated and stored in the register for each row readout step, to calculate the number of black pixels in each column.

After finishing calculation of $\sum_y p_{xy}$ (Y-direction) in each column, the sum of the each column's result is performed by sequential readout and accumulation for all the columns in order (X-direction) with enable signal for tri-state buffer, XSEL, to obtain $\sum_x \sum_y p_{xy}$, the area of the pupil. The result of $\sum_y p_{xy}$ in each column is readout through the connected data bus, S_n , in order for the adder and the register as shown in Fig. 8, which is located at outside the column array, as shown in Fig. 2.

3.3 Calculation of $\sum_x \sum_y x p_{xy}$

The circuit of calculating $\sum_y x p_{xy}$ at each column, which is indicated as "SX" in Fig. 3, has the similar configuration to that of Su described in section 3.2. Fig. 9 shows the one bit circuit of $\sum_y x p_{xy}$ calculation, SXu, as the element circuit to form the circuit with required number of bits. The product of the X-coordinate for each column and the binary flag data from the comparator, P , is accumulated by the similar architecture circuit of $\sum_y p_{xy}$ calculation. Note that this product of $x \cdot p_{xy}$ can be calculated by using the array of AND gate, since p_{xy} is equal to 0 or 1. The accumulation of all the columns is

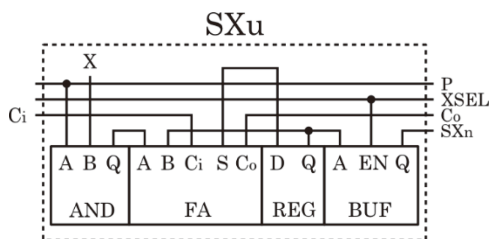


Fig.9 The 1-bit circuit of $\sum_y p_{xy}$ calculation, SXu.

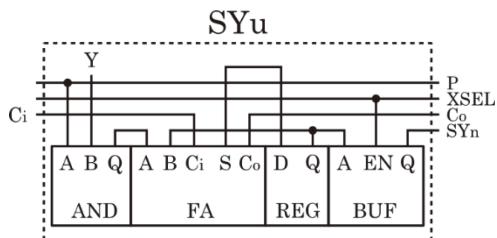


Fig.10 The 1-bit circuit of $\sum_y yp_{xy}$ calculation, SYu.

also performed with the same manner as $\sum_x \sum_y p_{xy}$ by the externally located accumulator.

3.4 Calculation of $\sum_x \sum_y yp_{xy}$

The circuit of calculating $\sum_y yp_{xy}$ at each column, which is indicated as "SY" in Fig. 3, also has the similar configuration of S and SX, described in section 3.2 and 3.3, respectively.

Fig. 10 shows the one bit circuit of $\sum_y yp_{xy}$ calculation, SYu, as the element circuit to form the circuit with required number of bits. The product of Y-coordinate and the binary flag data from the comparator, P, is calculated by using the AND gate array, and the sum of these products for all the column is calculated and accumulated by using adder array at each readout step for entire row.

After the accumulation, each values of $\sum_y yp_{xy}$ are accumulated for all the columns in X-direction by the circuit located outside the column array, and $\sum_x \sum_y yp_{xy}$ is obtained.

The centroid of the pupil can be calculated by eq. (1) with these three calculated results at each frame. Note that two division operations are required at each frame to obtain the centroid coordinates of the pupil, whose operation time and hardware overhead can be small enough compared to other processing steps.

4. Emulation on FPGA System

4.1 Hardware

We developed an emulation system composed of the high-speed camera (Lynx, IPX-VGA210-L) and FPGA (Xilinx, XC6SLX150-2FGG484C), as shown in Fig. 11, where the column-parallel processing architecture is



Fig.11 The developed emulation system composed of the high-speed camera and FPGA.

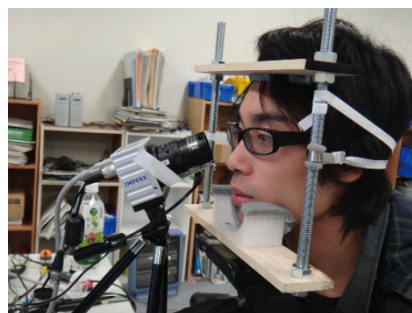


Fig.12 Setup of measurement experiment.

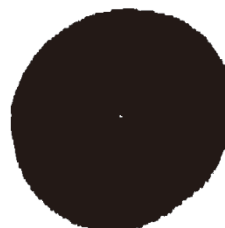


Fig.13 Observed pupil and the calculated centroid of the image.

implemented for algorithm evaluation.

4.2 Experiment

We confirmed the proper operation of the developed emulation system at the frame rate of 1,000[fps] with resolution of 640 x 64[pixels], as well as 500[fps] with 640 x 175[pixels] and 210[fps] with 640 x 480[pixels]. Note that the vertical resolutions of 64 and 175 are restricted by the camera's specifications at the frame rate of 1,000[fps] and 500[fps], respectively.

Fig. 12 shows setup of the experiment. The subject's head is fastened to a chin support to eliminate an effect by moving head, and illuminated from infrared LEDs. The camera with F2.8 lens including an infrared pass (visible light cut) filter captures the subject's eye from 5[cm] ahead.

Fig. 13 shows an observed infrared image of human's pupil, and a white point in the pupil indicates the centroid of the pupil area calculated by this emulation system.

4.3 Saccade Detection Experiment

We carried out a preliminary experiments to observe the eye movement by using the developed emulation system. The camera is set up to capture one subject's eye area, and the subject is required to read some horizontal sentences at 60[cm] ahead. **Fig.14** shows an example of the measured eye movement (X-coordinate of the pupil in the captured eye image) obtained from the emulation system operated at 500[fps], where the resolution is 640 x 175[pixels] due to the camera's specifications, where the leaping eye movement is observed. **Fig. 15** shows an example of the saccade movement extracted from Fig. 14.

We compared the another saccade measurement by using high-speed camera (CASIO EX-F1, frame rate of 1, 200[fps]) and the off-line image processing with the identical

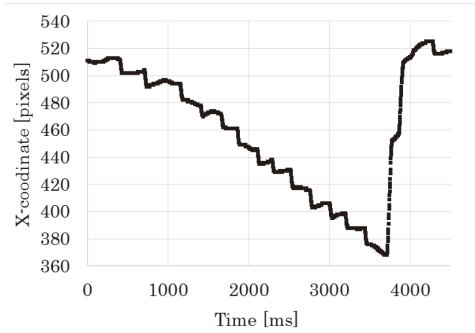


Fig.14 Measured eye movement using the developed emulation system.

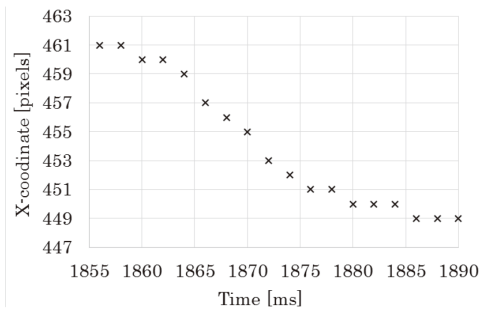


Fig.15 Extracted measured eye movement using developed emulation system.

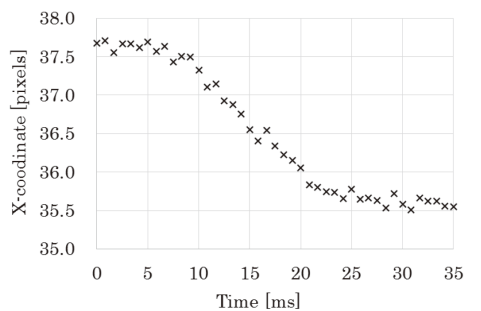


Fig.16 Measured eye movement using high-speed camera.

experimental condition to obtain the result of **Fig. 16**.

According to these two results, it was indicated that the saccade movement could be tracked by the column-parallel architecture implemented on the emulation system using high speed camera and FPGA.

5. Design of Integrated Image Sensor

We designed a preliminary LoS detection integrated image sensor with 16 x 16[pixels] using standard CMOS 0.18[um], five layers of metal technology, as shown in **Fig. 17**, **Fig. 18**, and **Fig. 19**. In this design, the size of the pixel is determined to be 10[um], which is equal to the width of the column processing circuits.

Note that the size of pixel plain is proportional to the resolution, N , while the size of the column-parallel

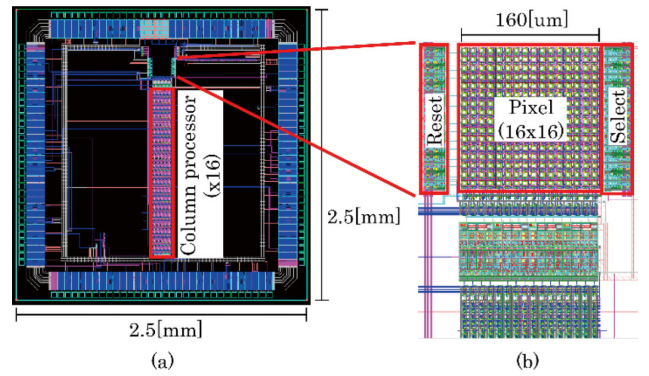


Fig.17 Layout of designed integrated image sensor. (a) Whole layout, (b) Image sensor section.

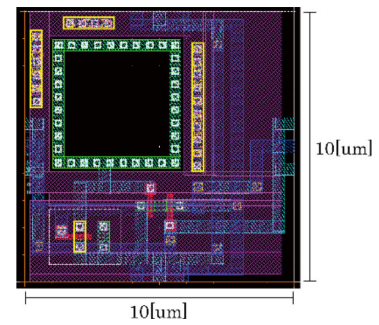


Fig.18 Layout of designed pixel circuit.

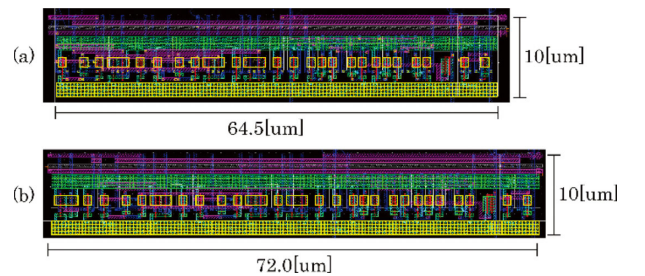


Fig.19 Designed column processing circuit. (a) $S_u (\sum_y p_{xy})$, (b) $S_{Xu} (\sum_y xp_{xy})$ and $S_{Yu} (\sum_y yp_{xy})$.

processing circuit is proportional to $\log_2 N$, and this indicates that the area of the LoS detection circuit becomes relatively smaller than the area of the pixel plain for the increased number of pixels, and the possibility of the high resolution LoS detection camera.

6. Conclusion

In this paper, we proposed the column-parallel architecture for LoS detection integrated image sensor based on centroid calculation.

We confirmed the proper operation of saccade eye tracking with the developed emulation system using high-speed camera and FPGA.

We also described the preliminary design of the integrated LoS calculation image sensor, and its evaluation will be reported in our future work.

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Hayato Kawakami received B.S. degree from School of Electrical and Computer Engineering, Kanazawa University in 2012, and currently in master course of Graduate School of Natural Science and Technology, Kanazawa University. His research interest is in an image sensor architecture with integrated image processing circuitry.



Satoru Igarashi received B.S. degree from School of Electrical and Computer Engineering, Kanazawa University in 2012, and currently in master course of Graduate School of Natural Science and Technology, Kanazawa University. His research interest is in an image sensor architecture with integrated image processing circuitry.



Yuta Sasada received B.S. degree from School of Electrical and Computer Engineering, Kanazawa University in 2013, and currently in master course of Graduate School of Natural Science and Technology, Kanazawa University. His research interest is in an image sensor architecture with integrated image processing circuitry.



Junichi Akita received B.S., M.S. and Ph.D. degrees in electronics engineering from the University of Tokyo, Japan in 1993, 1995 and 1998 respectively. He joined the Department of Computer and Electrical Engineering, Kanazawa University as a research associate in 1998. He moved to the Department of Media Architecture, Future University - Hakodate as an assistant professor in 2000. He moved to the Department of Information and Systems Engineering, Kanazawa University as an assistant professor in 2004. He has been an associate professor since 2008 in Kanazawa University, and currently a professor since 2011 in Kanazawa University. His main research interest is in analog parallel signal processing VLSI architecture and its applications. He is also interested in electronics systems including VLSI systems in the applications of human-machine interaction and human interface. He is a member of IEICE, IPSJ, and ITE.