Adiabatic SRAM with a large margin of VT variation by controlling the cell-power-line and word-line voltage

Adiabatic SRAM with a Large Margin of V_T Variation by Controlling the Cell-Power-Line and Word-Line Voltage

S. Nakata
Microsystem Integration Labs.
NTT
Atsugi 243-0198, Japan
nakata@aecl.ntt.co.jp

T. Kusumoto, M. Miyama and Y. Matsuda
Grad. School of Natural Sci. & Tech.
Kanazawa University
Kanazawa 920-1192, Japan
matsuda@ec.t.kanazawa-u.ac.jp

***Abstract*— An adiabatic 1-kb SRAM circuit was designed, which enables gradual charging during writing and reading while maintaining a large VDD so that the problems of V_T variation and electromigration in the nanocircuit can be resolved. In the writing mode, the voltage of the memory cell power line is reduced to ground gradually using a high-resistivity nMOSFET, and we turn off the nMOSFET so that the memory cell power line is set in a high-impedance state. Then, we can write data easily by inputting adiabatic signal from one bit line, while the other bit line is set to ground. For reading, a verifying operation is proposed for resolving the electromigration problem. The word line voltage is changed stepwise while the voltages of the bit lines are verified. The reading method enables a gradual current flow in the memory cell. We designed the cell layout and found that there is no area penalty. In addition, a new charge recycle circuit with tank capacitors is proposed.**

I. INTRODUCTION

Recently, the power consumption of LSIs has become very large. Reducing computation energy is therefore a serious issue. Particularly, the power consumed by SRAM circuits contributes dominantly to the total power consumption. Therefore, nanoscale SRAM circuits have been widely researched [1-4] for low-energy operation. In such SRAM circuits, the threshold voltage V_T varies very largely because the number of dopant atoms fluctuates statistically. This V_T variation would make it impossible for a nanoscale SRAM to write and read data.

To resolve the V_T variation problem in an SRAM, Zhang et al. proposed that the voltage of the memory cell power line (MCPL) be decreased when writing [1]. In another type of SRAM, the MCPL is cut off from the power line [2], and an improved version of that circuit achieves a decrease in the MCPL voltage [3]. These circuits are effective for increasing the margin of V_T variation when writing because the current drivability of external bit line (BL) signals is much stronger than that of a flip flop (FF). However, in these circuits, the MCPL voltage is almost equal to VDD, which is not very effective for resolving the V_T variation problem. The MCPL cannot be decreased to GND because the data of the unselected word line (WL) vanish if the MCPL is set to GND. The data vanish because the MCPL is shared with different words.

Recently, an adiabatic circuit has been proposed at the memory-cell level, in which the MCPL decreases to GND drastically [4]. This is very effective for resolving the V_T variation problem. The concept of an adiabatic SRAM is shown in Figs. 1(a) and (b). In this operation, the circuit does not need to invert the FF data forcibly. Instead, the voltage of the FF increases gradually from GND to a large VDD level according to the external BL voltage. Due to this gradual

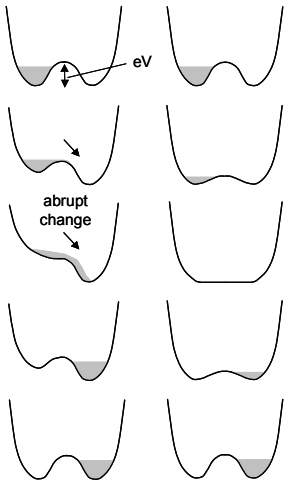

Table I. Scaling law.

parameter	scaling
L, W, t	K^{-1}
V	K^{-1}
E	1
I	K^{-1}
Wt	K^{-2}
J =I/(Wt)	K
τ =Wt/J^2	K^{-4}

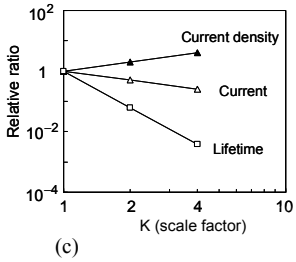

Fig. 1. Schematics of the (a) potential change of conventional SRAM and (b) that of adiabatic SRAM. (c) Wire lifetime determined by electromigration.

operation, the SRAM can also avoid the electromigration problem. Table I shows the physical parameters and scaling values under the constant electric field condition, where L, W, t, V, E, I, J, and τ are the length, width, thickness, power supply voltage, electric field, current, current density, and wire lifetime, respectively. The wire lifetime is written as $\tau=Wt/J^2$ so that τ becomes very small when the device size becomes small as shown in Fig. 1(c). The proposed SRAM can avoid the electromigration problem due to its gradual operation. Therefore, a 10-nm-node SRAM could be realized, which would make low-energy operation possible. In this work, we first designed an adiabatic 1-kb SRAM circuit at the layout level and confirmed that there is no area penalty and verified its low-current operation.

II. SRAM CIRCUIT STRUCTURE

The SRAM circuit in this work is shown in Fig. 2(a). The circuit uses a low-resistivity pMOS transistor S1 connected between the power line and MCPL, which is different from the previous adiabatic SRAM circuit [4]. Therefore, there is no large IR drop at the MCPL so that we can increase the static noise margin during reading. As before, the circuit uses a high-resistivity nMOS transistor S2 connected between the GND and MCPL. These switching transistors (S1 and S2) can be shared by many memory cells in one word in the row direction. Because of the sharing, the number of transistors in the cell can be reduced to about six. In this circuit, the MCPL voltage change is adiabatic and quasi-static because of

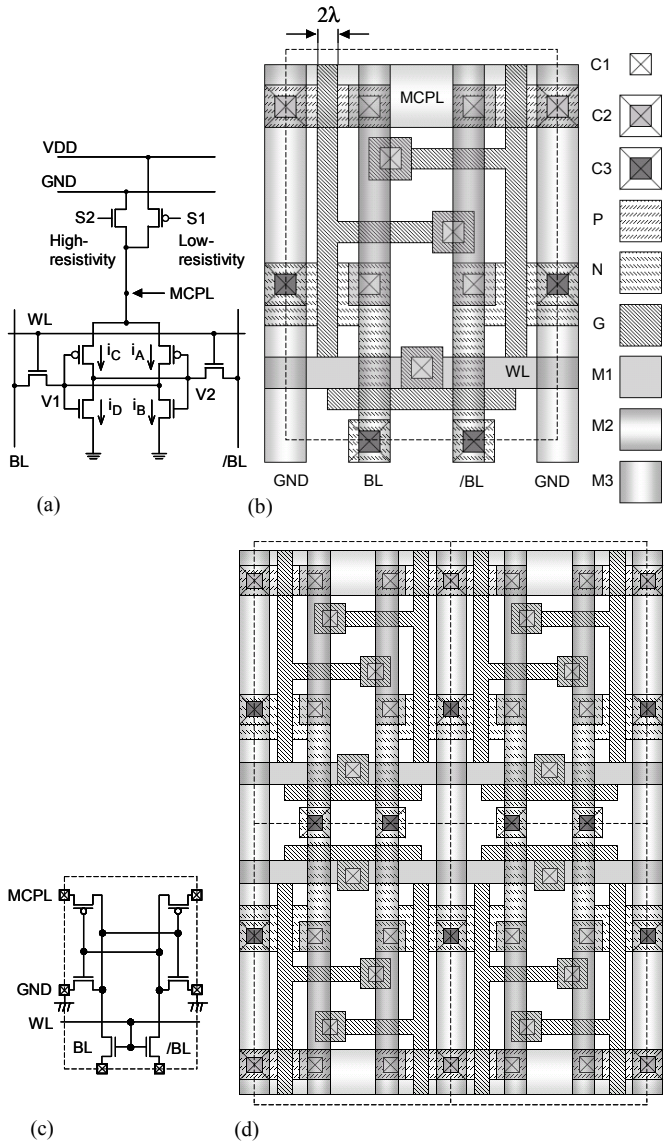

Fig. 2. Adiabatic SRAM circuit. (a) Circuit. (b) Layout. (c) Corresponding circuit of (b). (d) 2x2 cell layout.

the use of the high-resistivity switching transistor so that the electromigration problem can be resolved.

We used the memory cell circuit layout in Fig. 2(b). C1 (C2 or C3) is a contact between metal 1 (2 or 3) to the diffusion layer. P (N) is the P (N)-diffusion area. G is the gate area (poly-Si). M1 (M2 or M3) is the metal 1 (2 or 3) area. In Fig. 2(b), the MCPL and WL are set in the upper and lower side of the cell in the row direction, respectively. The GND and BL are set at the edge and center in the column direction, respectively. The corresponding circuit is shown in Fig. 2(c). The memory cell is arrayed as shown in Fig. 2(d), which is a 2×2 memory cell. In the layout, we can decrease the MCPL of the selected memory cell to GND because the MCPL is not shared with different words. As for the unselected memory cell, the MCPL maintains VDD so that the data information is maintained. We can decrease the MCPL to GND without losing the other data. This situation is far different from that in previous SRAM circuits [1-3], in

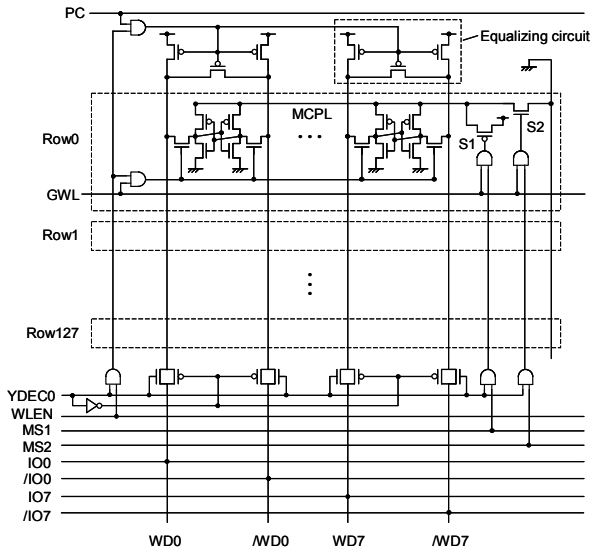

Fig. 3. Whole circuit with peripheral circuits.

which the MCPL can not be decreased to GND because the other data information would vanish. In Fig. 3, we show the whole circuit, including switching transistors S1 and S2 and the peripheral circuits. The SRAM is composed of 128 words and one word is composed of 8 bits. Here, to decrease the area penalty, S1 and S2 are shared by one word.

III. SIMULATION RESULTS

The SRAM was simulated using SPICE. We used the 0.18-μm design rule. However, adiabatic charging operation would be expected to resolve the electromigration problem even with 10-nm technology.

VDD was 1.8 V. V_T's were 0.43 and −0.33 V in nMOS and pMOS, respectively. The body biases of nMOS and pMOS are GND and VDD, respectively. The simulation result is shown in Fig. 4. VS1(VS2) is the gate voltage of S1 (S2). First, when t=0 ns, VS1 and VS2 are low so that the MCPL is connected to VDD. When t=4 ns, VS1 and VS2 become high so that the MCPL is connected to GND. At this time, the coupling currents of i_A and i_D flow according to the change of VS1 and VS2. After the MCPL is connected to GND, the MCPL voltage decreases gradually to zero due to the high resistivity of S2. In addition, the high node of the FF, V1, decreases gradually to the V_T level. When t=8 ns, VS2 becomes low so that the MCPL is not connected anywhere and is therefore in a high-impedance state. This situation is the same as that in other proposed SRAM circuits [2-3]. However, the MCPL voltage in our circuit is at the GND level, not at the VDD level. When t=9 ns, the WL voltage becomes high so that the transfer transistors are activated and the FF is connected to the BLs. At this time, V1 is decreased from V_T to GND. Then, the /BL voltage increases gradually from GND to VDD, while the BL voltage is set to GND. The FF node voltage of V2 increases gradually according to the /BL, while V1 stays low. The MCPL voltage also increases gradually according to the /BL. From Fig. 4, it is clear that operation at about 100 MHz is possible in the SRAM. Regarding current, the maximum value is 6 μA. The current value for charging the FF (i_C at

t=10 ns) is the same order as the coupling current (i_A and i_D at t=5 ns). This means the charging current of the FF from the /BL is very small and negligible.

Fig. 5 shows the simulation for the conventional SRAM. At t=10 ns, the FF data are inverted. The maximum current flow is 100 μA (i_D), which is 16 times larger than that of the adiabatic SRAM. For comparison of the wire lifetime between the adiabatic and the conventional SRAM, we consider the value r, which is defined as the integral of I^2 as a function of t. From Figs. 4 and 5, r is calculated regarding i_A to i_D, respectively. By averaging r from i_A to i_D, we can expect that τ in the adiabatic SRAM would be about 120 times longer than that in the conventional one.

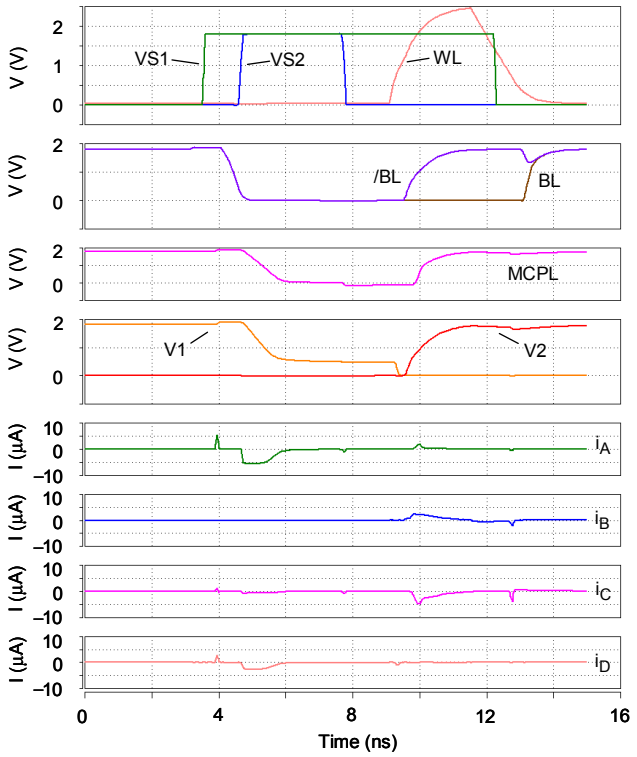

Fig. 4. Simulation results for adiabatic SRAM during writing.

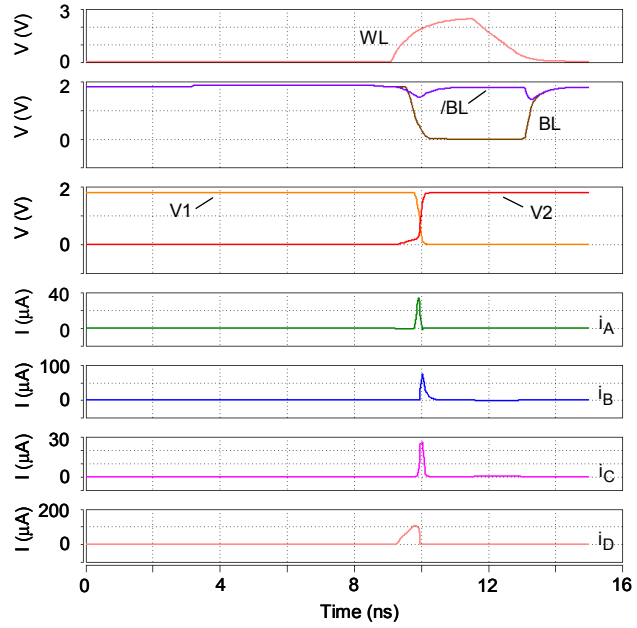

Fig. 5. Simulation results for conventional SRAM during writing.

IV. VERIFYING OPERATION

Here, we consider the reading mode. The circuit is shown in Fig. 6. First, all BLs are precharged to VDD. Then, the WL is set from GND to V_1; for example, 1/4 · VDD. If we can detect the voltage reduction of a certain BL due to the GND node of a FF, we can know that the BL data value is low. To detect the voltage reduction, we used latch-type sense amplifiers, which are set at each BL and /BL. Then, using a buffer, we discharge to GND only the BL in which we detected the voltage reduction. In the next stage, the WL is increased to V_2; for example, 2/4 · VDD. Again, we sense the states of the BLs. As for the previous BL set to GND, current no longer flows. As for the other BLs, again, we detect the voltage reduction. By repeating this process, we can decrease the current from the BL to the FF. Fig. 7 shows the timing chart of the reading mode. As pointed out earlier, WL increases stepwise monotonically, which is different from the previous work [4]. Here, V_{T1} and V_{T2} are the V_T's of the transistors connected to BL1 and BL2, respectively.

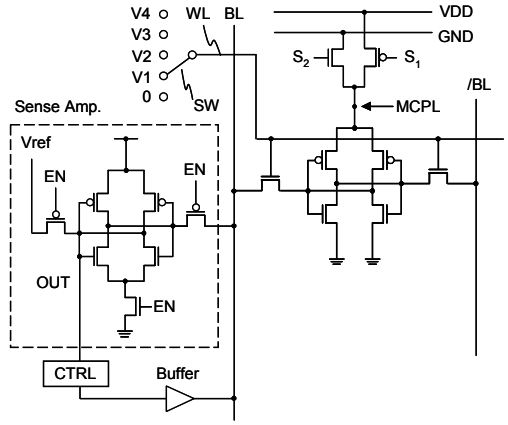

Fig. 6. Verifying circuit during reading. The value of Vi is i/4 × VDD. CTRL means controller.

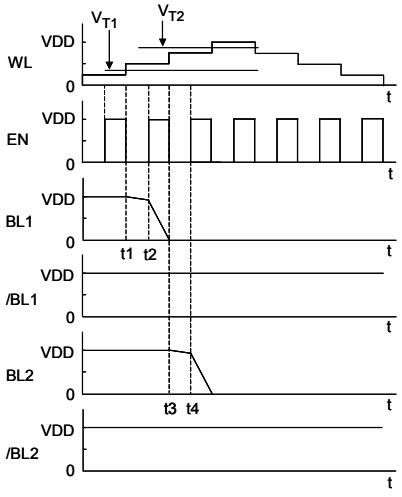

Fig. 7. Timing chart during reading.

If the WL becomes larger than V_{T1} at t=t1 and the BL1 data value is low, the BL1 voltage decreases gradually. At t=t2, we can detect the voltage drop with a sense amplifier. Then, we can discharge the charge in BL1 using the buffer in Fig. 6. Therefore, we can avoid large current flow into the cells.

Fig. 8 shows the simulation result in the four-step verifying mode. We set the V_T values to 0.43, 0.83, and 1.40 V as parameters, taking the V_T variation into consideration. I_1 (I_2 or I_3) is the current from the BL to the FF when V_T is equal to V_{T1} (V_{T2} or V_{T3}). Fig. 9 shows the simulation in the conventional mode for comparison. I_1 (I_2 or I_3) is the same as before. In Fig. 9, when V_{T3}=1.40 V, the BL voltage decreases to 1.6 V, which is the same value as in Fig. 8. Therefore, the comparison of the maximum current between Figs. 8 and 9 is fair. As before, the integral of I^2 as a function of t is calculated. As a result, it is found that the wire lifetime in the four-step verifying mode is ten times longer than that of the conventional SRAM.

The V_{T3} value of 1.40 V is thought to be very large. However, since the circuit is not under the subthreshold operation, the gate delay time would not be large. Although

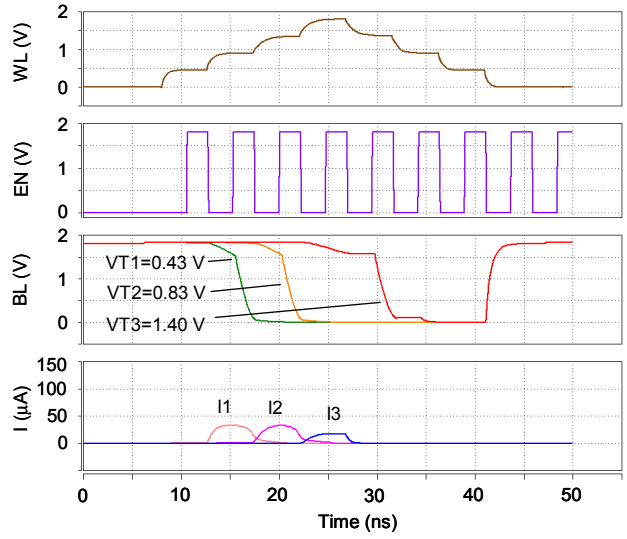

Fig. 8. Simulation of verifying operation during reading.

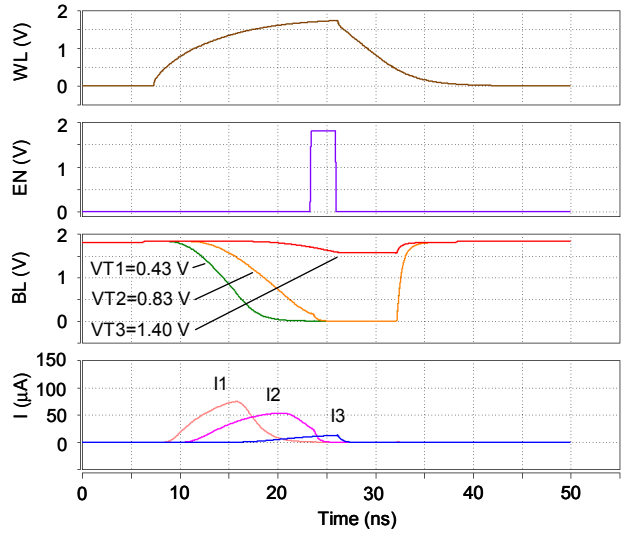

Fig. 9. Simulation results for the conventional during reading.

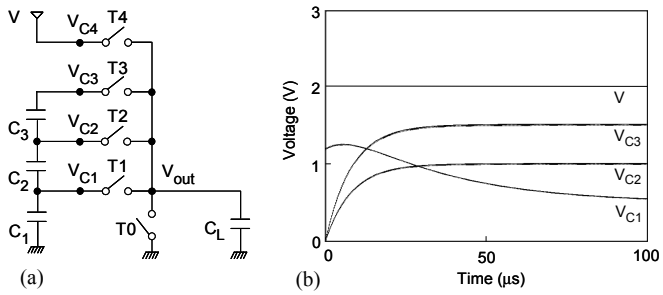

Fig. 10. New charge recycle circuit with tank capacitors. (a) Circuit. (b) Simulation results.

the delay time of the BL with V_{T3}=1.40 V in Fig. 9 is very large due to the large BL capacitance, the delay time of logic gate would be less than 5 ns.

The above verifying operation makes the operation slow. In this case, throughput can be increased by parallel operation, such as 128 bits or more. In general, parallel operation is important in nanocircuits.

To achieve the verifying operation, stepwise voltage is necessary. Here, a new circuit that produces stepwise voltage is proposed, which is shown in Fig. 10(a). T0, T1, T2, T3, T4, T3, T2, and T1 turn on successively and this operation is repeated. There are three tank capacitors, the same as in the circuit in [5], while there are four in the circuit in [6]. This means that we can make the circuit as compact as the one in [5]. The simulation is shown in Fig. 10(b). Stepwise voltage is spontaneously generated. The stabilization can be explained by using the matrix theory of the eigenvalue [6].

V. CONCLUSION

In summary, we designed a new adiabatic 1-kb SRAM, in which there is almost no area penalty. After the voltage of the memory cell power line is set to GND and enters a high-impedance state, it is adiabatically charged from the BL during writing. For reading, the WL voltage is changed stepwise monotonically while the BL voltages are verified. With a large VDD value and the gradual charging, the SRAM can avoid the problems of V_T variation and electromigration. In addition, a new charge recycle circuit is proposed for producing stepwise voltage.

REFERENCES

[1] K. Zhang et al., "A 3-GHz 70Mb SRAM in 65nm CMOS Technology with Integrated Column-Based Dynamic Power Supply," in *Proc. ISSCC Dig.*, pp.474-475, Feb. 2005.

[2] M. Yamaoka et al., "Low-power embedded SRAM modules with expanding margins for writing," in *Proc. ISSCC Dig.*, pp.480-481, Feb. 2005.

[3] S. Ohbayashi et al., "A 65 nm SoC Embedded 6T-SRAM Design for Manufacturing with Read and Write Cell Stabilizing Circuits," in *Proc. Symp. VLSI Circuits Dig.*, pp.17-18, June 2006.

[4] S. Nakata, "Adiabatic SRAM with the large margin of V_{th} variation by the gradual change of the voltage," *IEICE Electron. Express*, vol. 3, pp.304-309, July 2006.

[5] L. J. Svensson and J. G. Koller, "Driving a capacitive load without dissipating fCV^2," in *Proc. IEEE Symp. Low Power Electronics Dig.*, pp.100-101, Oct. 1994.

[6] S. Nakata, "Stability of adiabatic circuit using asymmetric 1D-capacitor array between the power supply and ground," *IEICE Electron. Express*, vol. 4, pp.165-171, Mar. 2007.